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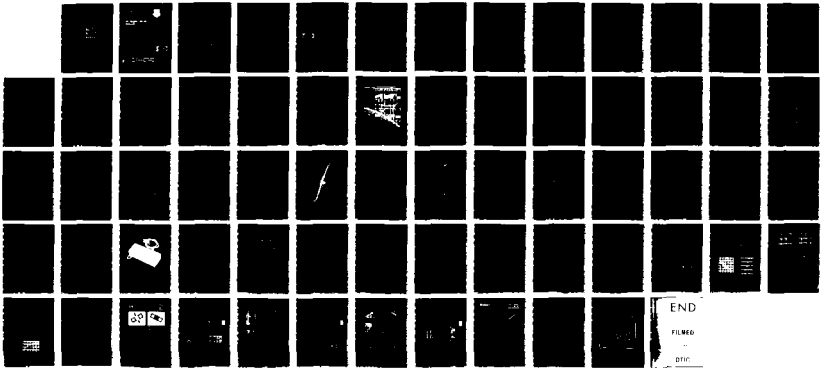

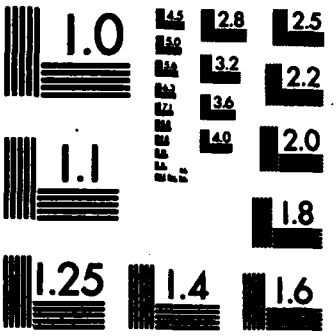

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RADC-TR-84-117
Final Technical Report
June 1984

AD-A147 715

EMC ENHANCED CONSTANT "Z" MODULATOR

ITT

R. E. Reed

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, NY 13441

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APPROVED: Thomas E. Baustert

THOMAS E. BAUSTERT
Project Engineer

APPROVED: W. S. Tuthill

W. S. TUTHILL, Colonel, USAF
Chief, Reliability & Compatibility Division

FOR THE COMMANDER: John A. Ritz

JOHN A. RITZ
Acting Chief, Plans Office

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The EMC Enhanced constant "Z" modulator (EECZM) research and development effort at ITT-A/OD was undertaken to provide an amplitude modulation capability for a low-noise, medium power (1 Watt), wideband (225-400 MHz), frequency hopping (1000 hops/sec) synthesizer currently in development at the ITT-A/OD facility for RADC. The primary objective was to amplitude modulate the synthesizer's RF carrier to the required modulation percentage while avoiding frequency modulation of the RF carrier

AN RF carrier amplitude modulator can seriously degrade synthesizer noise performance through modulator impedance changes during the modulation cycle. This change in impedance causes frequency modulation of the synthesizer's voltage controller oscillator (VCO) resulting in RF carrier FM sidebands extending far beyond the AM sidebands for a large modulation index. Usually the modulator is isolated from the VCO by 20 to 30 dB of buffer amplification to minimize VCO frequency modulation; however, buffer amplifiers tend to degrade

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the overall synthesizer noise performance. By controlling the modulator's impedance to the VCO during the modulation cycle, the VCO buffer stages can be omitted while RF carrier frequency modulation is minimized.

The program approach centered about reviewing a previous IR&D effort at ITT-A/OD relating to a constant impedance amplitude modulation scheme and culminated in a breadboard, and ultimately a feasibility model, to meet the modulator's statement-of-work (SOW) requirements

A major portion of the R&D effort focused on design and test of the modulator's constant impedance attenuator. Several modulator designs were modeled resulting in adoption of a hybrid coupler/PIN diode attenuation scheme. This type of modulator impresses audio modulation onto the synthesizer's RF carrier via PIN diodes terminating a hybrid coupler while providing a constant impedance to the VCO during the modulation cycle.

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ABSTRACT

This final report covers the design concept and feasibility model for a UHF-medium power (2 watts) EMC Enhanced Constant "Z" Modulator (EECZM). The program augments an on-going developmental effort at ITT-A/OD of a low-noise medium power wideband (225-400 MHz) frequency hopping (1000 hops/sec) synthesizer. The deliverable feasibility model meets, or exceeds, all critical design parameters when tested as a stand-alone equipment or while modulating the low-noise synthesizer's RF carrier.

Final Report
For
EMC Enhanced Constant "Z" Modulator

Section 1

1.1 Introduction

This final report describes the theory, design, and evaluation of an EMC Enhanced Constant "Z" Modulator (EECZM) feasibility model designed to operate in conjunction with a low-noise, UHF frequency hopping synthesizer. The EECZM impresses amplitude modulation onto an RF carrier (225-400 MHz) via hybrid coupler-PIN diode attenuator. The EECZM presents a constant source impedance to prevent incidental frequency modulation. Automatic level control (ALC) guarantees that the modulation percentage is independent of the carrier amplitude.

1.2 Program Description

The program was initiated with the design, construction, and test of critical modulator circuitry. Optimization of the modulator breadboard led to a redesign of the modulator from a controlled PIN diode arrangement to a hybrid coupled isolated PIN diode configuration. Successful modulator breadboard test results were the basis for the construction and test of the modulator feasibility model. The model was evaluated for such critical parameters as insertion loss, source frequency pulling, source signal-to-noise degradation and modulation percentage as a function of input frequency. The feasibility model tests proved the success of the program.

1.3 Report Organization

The EECZM final report is organized as shown:

Section 2	EECZM Requirements - The EMC Problem
Section 3	Program Technical Approach
Section 4	Program Final Test
Section 5	Conclusions and Recommendations
Section 6	Appendix

1.4 Modulator Specifications

Table 1.4-1 lists the modulator's goals and specifications as delineated in the program's statement of work (SOW).

Table 1.4-1. Constant "Z" Modulator Goals and Specifications

PARAMETER	SPECIFICATION	GOAL
Frequency Range	225 to 399.975 MHz	
Input Power	30-33 dBm	
Insertion Loss	<4 dB	
Input Impedance	50Ω Nominal	VSWR ≤2:1
Output Impedance	50Ω Nominal	VSWR ≤2:1
Output Signal-to-Noise Degradation	≤6 dB	≤3 dB
Incidental FM	<2.5 kHz	
Modulation Frequency (3 dB Bandwidth)		
Narrowband	300 Hz to 3.5 kHz	Nominal
Wideband	300 Hz to 25 kHz	Nominal
Minimum Modulation Capability		
Narrowband (1 kHz at 1.4 Vrms)	+85% - 90%	
Wideband (1 kHz at 12 V_{pp})	+85% - 90%	
Distortion (90% Negative Modulation)	10%	5%
Modulation Input Impedance		
Narrowband		
Balanced	150Ω ± 20%	
Unbalanced	150Ω ± 20%	
Wideband		
Balanced	6000Ω ± 10%	
Unbalanced	2000Ω ± 10%	

Section 2

AMPLITUDE MODULATOR SYSTEM REQUIREMENTS - THE EMC PROBLEM

Receiver degradation caused by off-channel transmitters is a problem that has been recognized since the early days of radio. The use of solid-state technology in modern communications equipment has, in many cases, made the problem more severe. The low-noise, crystal oscillator has been replaced by the noisy digital synthesizer. The narrowband, vacuum-tube power amplifier has been replaced by a solid-state power amplifier with bandwidths and noise that covers many octaves. The vacuum-tube receiver has given way to the solid-state receiver that, in many cases, has inferior signal handling capabilities. High-Q, mechanically-tuned preselectors are being replaced by varactor-tuned filters, which not only have less selectivity, but also generate additional distortion. At the same time, the number of radio systems has increased and user requirements often dictate collocated operation. The receiver degradation caused by noise and off-channel signals is often referred to as desensitization, one of the major electromagnetic compatibility (EMC) problems.

Transmitter noise poses a particularly difficult problem because output noise is broadband. Unlike a transmitter spurious output broadband noise can degrade performance over a wide frequency range rather than a single channel. The output noise of a transmitter can only be minimized by generating the carrier with a high power oscillator in the synthesizer so that the required gain of the stages following the oscillator is minimized. Low level, low-noise oscillators followed by several stages of gain to produce the required transmitter output power is not a viable approach because the noise contributed by the gain stages degrades the noise performance of the transmitter.

The phase noise associated with a VCO occurs at frequencies near the carrier and hence can not easily be reduced by filtering. Care must be taken in the overall design of a transmitter so that phase noise is held to a minimum.

An amplitude modulator can seriously degrade synthesizer noise performance because the impedance of the modulator changes during the modulation cycle. This change in impedance causes frequency modulation of the Voltage Controlled Oscillator (VCO) in the synthesizer. The FM sidebands can extend beyond the AM sidebands if the modulation index is large.

Experience with this problem at ITT-A/OD has shown that even 20 or 30 dB of isolation between the modulator and the VCO may not be sufficient to reduce the frequency modulation to acceptable levels and that isolation, along with a reduction of the impedance changes in the modulator, is required to reduce the frequency modulation of the VCO to an acceptable level. Therefore, isolation provided by a buffer amplifier and an isolator will not reduce the frequency modulation of the VCO sufficiently to meet the specifications of the EECZM.

The technique of using high-level oscillators and minimum gain following the oscillator to minimize transmitter output noise makes it more difficult to control frequency modulation of the oscillator because there is less isolation between the oscillator and the modulation than in a transmitter using a low-level oscillator.

Section 3

TECHNICAL APPROACH

There are several ways to amplitude modulate a transmitter. The modulation process can be incorporated into a feedback system or it can be accomplished without feedback. An example of the latter technique is to apply the modulating signal to the collectors of the final amplifier and its driver stage. This technique requires a high-power modulator, but the RF amplifiers do not have to be linear. This type of modulation can also be used with the low-power amplifier in the transmitter, but then all stages following the last modulated stage must be linear to preserve the modulation envelope. Modulation can also be applied to the bases of the transistors in the RF amplifier chain, but again all stages following the modulated stages must be linear. In either case, the input impedance of the transistors will change during the modulation cycle and cause incidental FM because the synthesizer is not presented with a constant load impedance.

Another technique uses a 90° hybrid with one of the output ports connected to a device like a PIN diode, which has its impedance change with the modulating signal. The other output port is connected to the antenna terminal or power amplifier. One of the input ports is connected to a matched load while the other is connected to the driver stage. Two cascaded hybrid modulators are required to achieve a high percentage modulation because the isolation of the hybrid over the 225 to 400 MHz band is only about 20 dB. Although this technique offers a reduction in impedance change with modulation, it will not meet the requirements of the EMC Enhanced Constant "Z" Modulator.

Any of these techniques can be used with a feedback loop to reduce distortion. With a feedback loop, the stages following the modulated stage do not have to be linear. However, they will not meet the EECZM requirements because the change in input impedance is too large.

3.1 SYSTEM ANALYSIS

The ITT-A/OD approach utilizes an electronically controlled constant impedance attenuator in the transmitter signal path. See Figure 3.1-1.

To minimize the noise performance degradation caused by the attenuator, a buffer amplifier preceeds the attenuator. The gain of the buffer amplifier is equal to the loss in the attenuator so that with a 30 dBm input from the synthesizer, the output of the attenuator is 30 dBm. If the buffer amplifier followed the attenuator, the noise-to-signal ratio at the output of the modulator would be greater than that allowed by the total system.

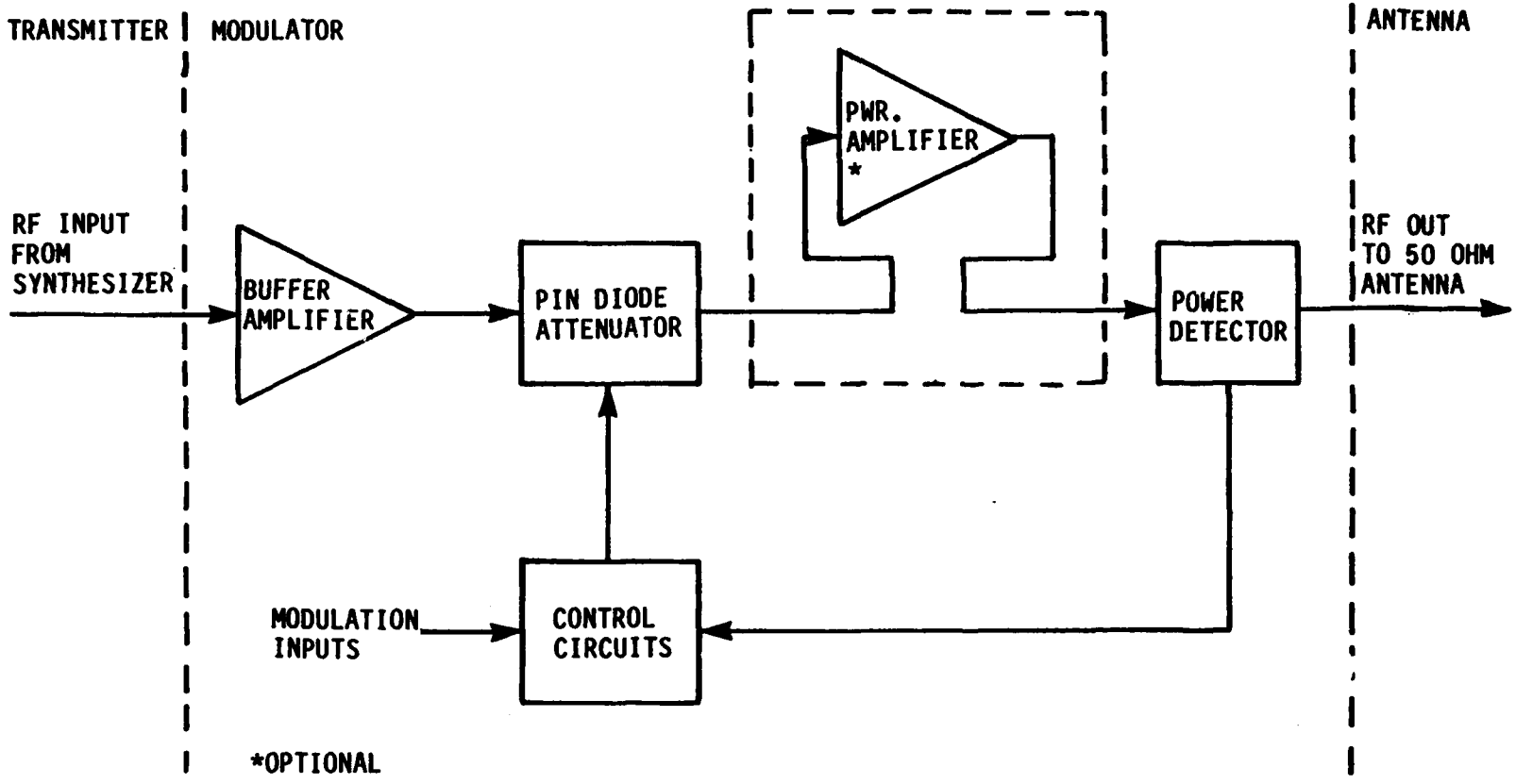


Figure 3.1-1. Block Diagram of a Transmitter Driving the Constant Z Modulator

The input impedance of the PIN diode attenuator must remain constant over the modulation cycle to ensure that the synthesizer is relatively free of incidental FM.

Automatic level control (ALC) is also incorporated into the design of the modulator. The power detector samples the output signal and the detected sample is used for linearizing the modulator and ALC. Provision is also made for adding a power amplifier inside the feedback loop. The modulator has been integrated into the design of a transmitter rather than just being an add-on to the synthesizer.

PIN diodes are used as the controlled circuit elements in the Constant Z variable attenuator. The only critical consideration when choosing the PIN diodes is the carrier lifetime. The carrier lifetime must be long when compared with the time for an RF cycle, but short when compared with the time for one cycle at baseband. The PIN diode must have a carrier lifetime on the order of 0.6 μS. These diodes are readily available.

3.1.1 Modulation Analysis

The baseline modulator is an electronically controlled attenuator that modulates the carrier by controlling the carrier amplitude. The carrier must be attenuated with no modulation applied so that upward modulation is produced by reducing the attenuation. For example, for 100-percent upward modulation, the unmodulated carrier must be attenuated 6 dB because the peak envelope power of a 100-percent amplitude modulated signal is 6 dB larger than the unmodulated carrier. The attenuation required for any modulation index, m, for upward modulation is:

$$\alpha_u = 20 \text{ LOG } (m + 1) \qquad (1)$$

This is the amount that the unmodulated carrier must be attenuated.

The attenuation required for any modulation index (m), for downward modulation is:

$$\alpha_D = \alpha_u - 20 \text{ LOG } (1-m) \qquad (2)$$

For 100-percent downward modulation, infinite attenuation is required to reduce the modulation envelope to zero; therefore, 100-percent downwards modulation is not possible with this type of modulator.

To meet the 85% positive and 90% negative modulation specifications required, α_u is 5.34 dB and α_D is 25.34 dB. Because most military radios are designed for 95-percent modulation, the EMC Enhanced Constant "Z" modulator is designed to accommodate 95-percent positive and negative modulation, in which case α_u = 5.8 dB and α_D = 31.8 dB. To provide ALC, additional attenuation is needed so that α_u = 8.0 dB and α_D = 34 dB.

3.1.2 Incidental FM Analysis

Incidental FM is caused by the change in load impedance during the modulation cycle that is presented to the oscillator in the synthesizer. The change in load impedance causes the instantaneous frequency of the oscillator to change with the changing input impedance of the modulator. The amount of frequency deviation depends on the oscillator circuit design, on the amount of isolation between the oscillator and the modulator, and on the change in input impedance of the modulator.

The sidebands generated in this frequency modulation process can extend far beyond the AM sidebands if the frequency deviation is large. Close-in sidebands will be reduced by the synthesizer if they fall within the loop bandwidth of the synthesizer. However, sidebands that fall outside the loop bandwidth of the synthesizer are not reduced.

Breadboard* measurements showed that even 30 dB of isolation is not sufficient to reduce the incidental FM to an acceptable level unless a constant impedance modulator is used.

3.1.3 Noise Analysis

The noise performance of the EMC synthesizer will be degraded by the modulator because any circuit following the synthesizer will add noise. The following analysis describes the mathematics of the degradation and shows how the added noise is held to a minimum. The noise model for the modulator is shown in Figure 3.1.3-1. The noise at the output of the modulator is:

$$N_O = G_1G_2N_i + (F_1-1)\, G_1G_2kT_o + G_2\, (F_2-1)\, kT_o \qquad (3)$$

and the carrier power is given by:

$$S_o = S_iG_1G_2 \qquad (4)$$

where:

G_1 is the gain of the buffer amplifier
G_2 is the gain of the modulator
F_1 is the noise figure of the buffer amplifier
F_2 is the noise figure of the modulator
k is Boltzmann's constant
T_o is 290K and
N_i/S_i is the noise-to-signal ratio of the synthesizer

Because the modulator is an attenuator, its noise figure is the attenuation (α), and its gain is $1/\alpha$.

*Previous ITT-A/OD IR&D program.

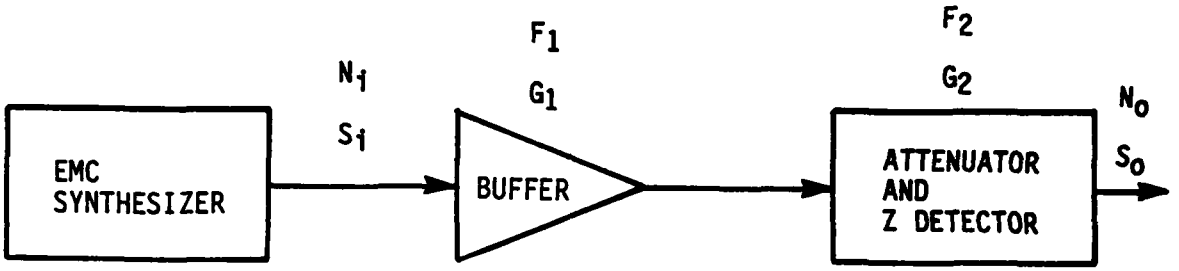


Figure 3.1.3-1. Noise Model for the Modulator

Dividing (3) by (4) yields:

$$\frac{N_o}{S_o} = \frac{N_i}{S_i} + \frac{(F_1 - 1)\, kT_o}{S_i} + \frac{(\alpha - 1)\, kT_o}{S_i G_1} \qquad (5)$$

With $\alpha = 8$ dB, $G_1 = 8$ dB, and $S_i = 30$ dBm, (5) becomes:

$$\frac{N_o}{S_o} = \frac{N_i}{S_i} + (F_1 - 1)\, kT_o + .842\, kT_o \qquad (6)$$

The noise-to-signal ratio specification for the synthesizer at $\pm$ 10 MHz is -198 dbc/Hz. The noise-to-signal ratio at the output of the modulator is then:

$$\frac{N_o}{S_o} = 4 \times 10^{-21} (F_1 - 1) + 1.92 \times 10^{-20} \qquad (7)$$

At $\pm$ 5 MHz, the noise-to-signal ratio of the synthesizer is -195 dBc/Hz and the noise-to-signal ratio at the output of the modulator is:

$$\frac{N_o}{S_o} = 4 \times 10^{-21} (F_1 - 1) + 3.50 \times 10^{-20} \qquad (8)$$

At $\pm$ 0.5 MHz, the noise-to-signal ratio of the synthesizer is -180 dBc/Hz and at the output of the modulator:

$$\frac{N_o}{S_o} = 4 \times 10^{-21} (F_1 - 1) + 10^{-18} \qquad (9)$$

At $\pm$ 20 kHz, the noise-to-signal ratio of the synthesizer is -145 dBc/Hz and at the output of the modulator:

$$\frac{N_o}{S_o} = 4 \times 10^{-21} (F_1 - 1) + 3.16 \times 10^{-15} \qquad (10)$$

The greatest degradation in output noise-to-signal ratio occurs at $\pm$ 10 MHz. Figure 3.1.3-2 is a plot of the output signal-to-noise ratio at the output of the modulator for $\pm$ 10 MHz frequency offsets. Here, at the synthesizer output, the noise-to-signal ratio is -198 dBc/Hz. For a 3 dB degradation, the noise figure of the buffer amplifier must be no larger than 6 dB. For a 6 dB degradation, the noise figure of the buffer amplifier can be as large as 11 dB.

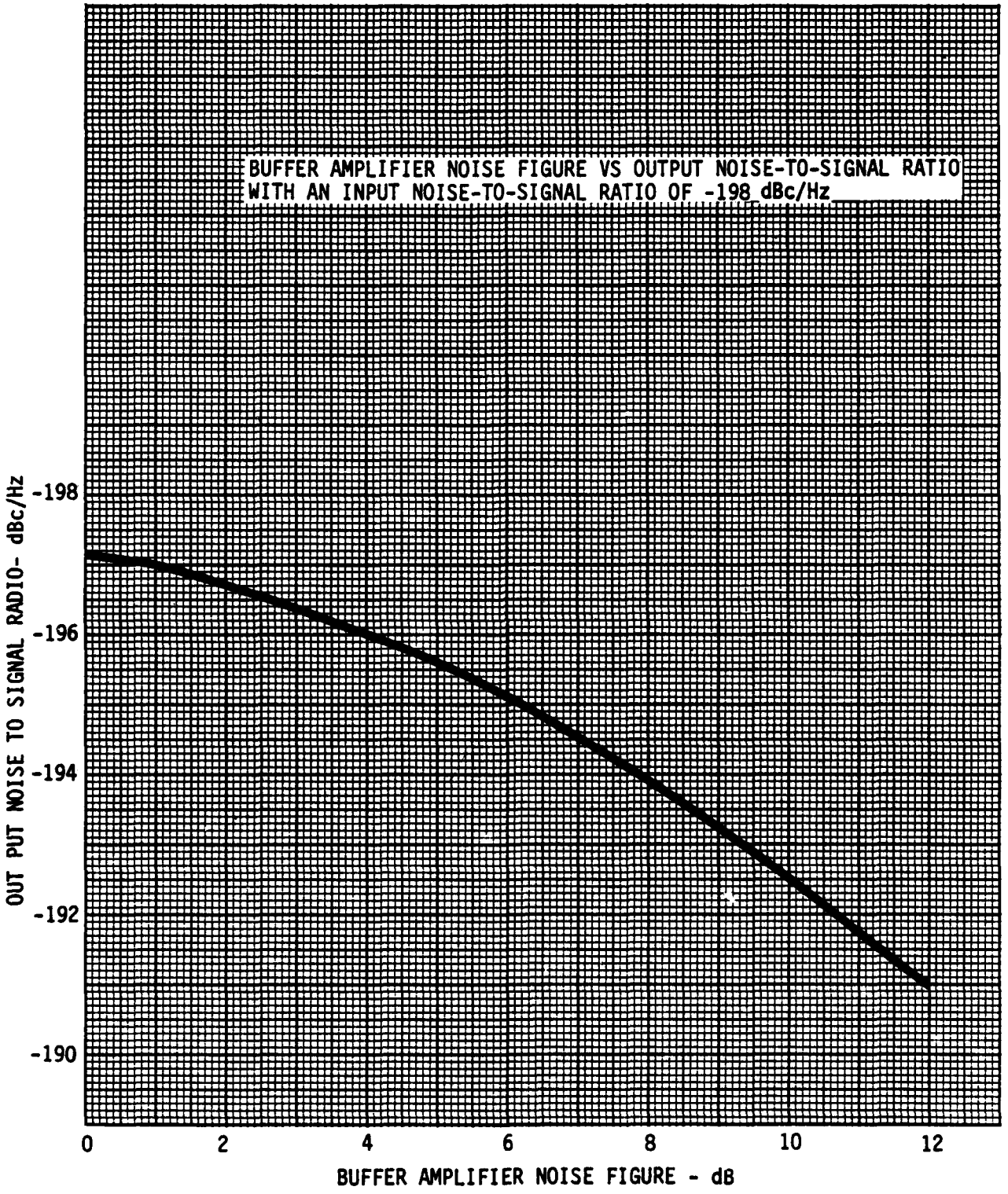


Figure 3.1.3-2. Buffer Amplifier Noise Figure Versus Output Noise-to-Signal Ratio

Table 3.1.3-1 shows the degradation in output noise-to-signal ratio caused by the modulator at the four specified frequency offsets for both a 6 dB and 11 dB buffer amplifier noise figure.

Table 3.1.3-1 N/S Degradation/dB.

Buffer Amplifier Noise Figure/dB	± 20 KHz	± 0.5 MHz	± 5 MHz	± 10 MHz
6	0	0.1	1.7	3
11	0	0.2	4.1	6

3.2 Modulator Design

Figure 3.1-1 is a block diagram of the feasibility modulator model. Figure 3.2-1 is a detailed schematic of the modulator. The individual blocks and their schematic representations are described in this section.

3.2.1 Buffer Amplifier

The buffer amplifier located at the modulator's RF input port provides an 8 dB nominal gain across the 225-400 MHz band.

It was shown in paragraph 3.1.1 that 8 dB of attenuation is required for modulation. To overcome this loss the buffer amplifier must have a gain of 8 dB.

Because the modulator must present a VSWR of <2:1 to the synthesizer the modulator's input impedance must be well controlled. The buffer amplifier isolates the PIN diode attenuator's input VSWR variations as the attenuator impresses amplitude modulation onto the RF carrier.

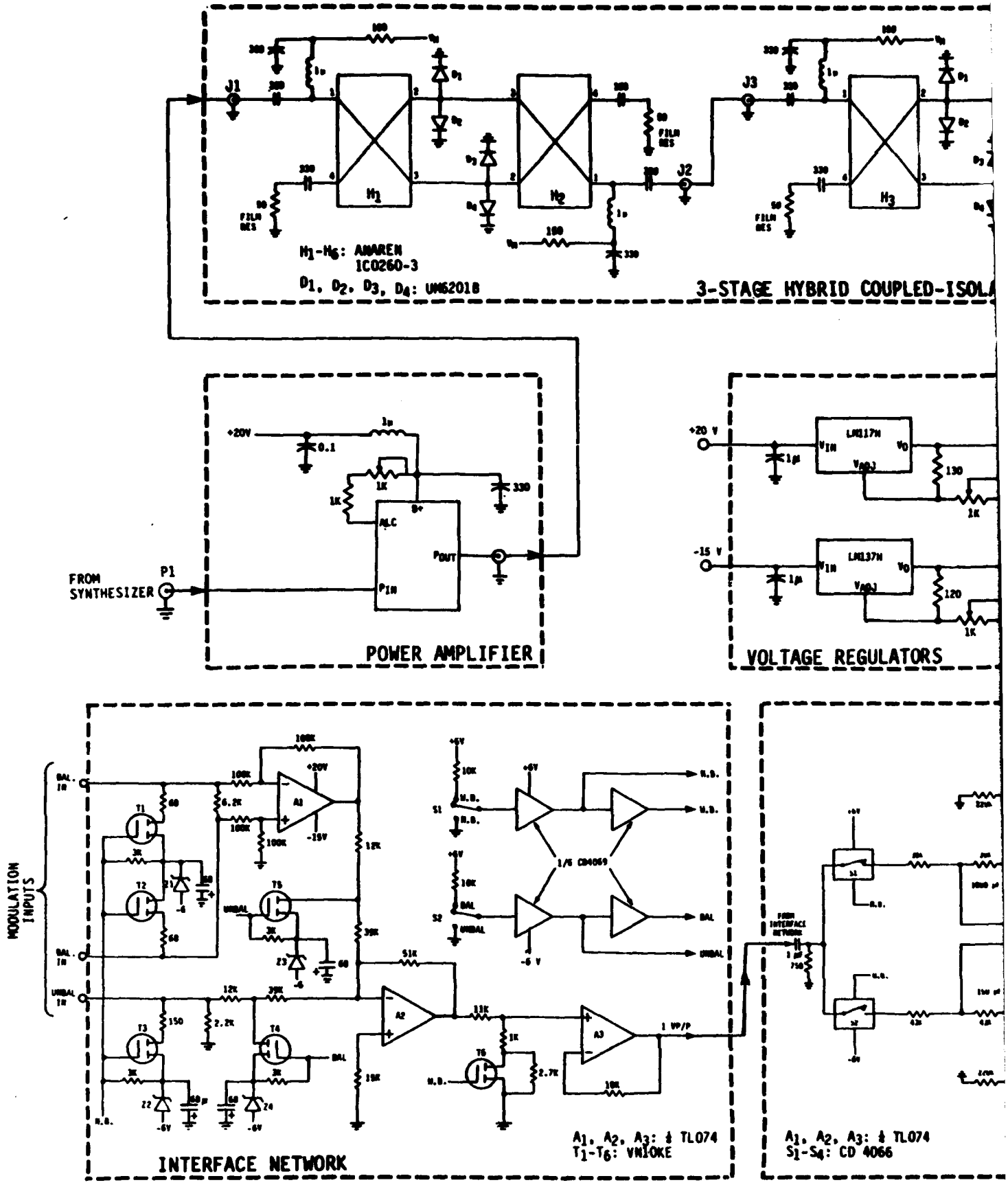
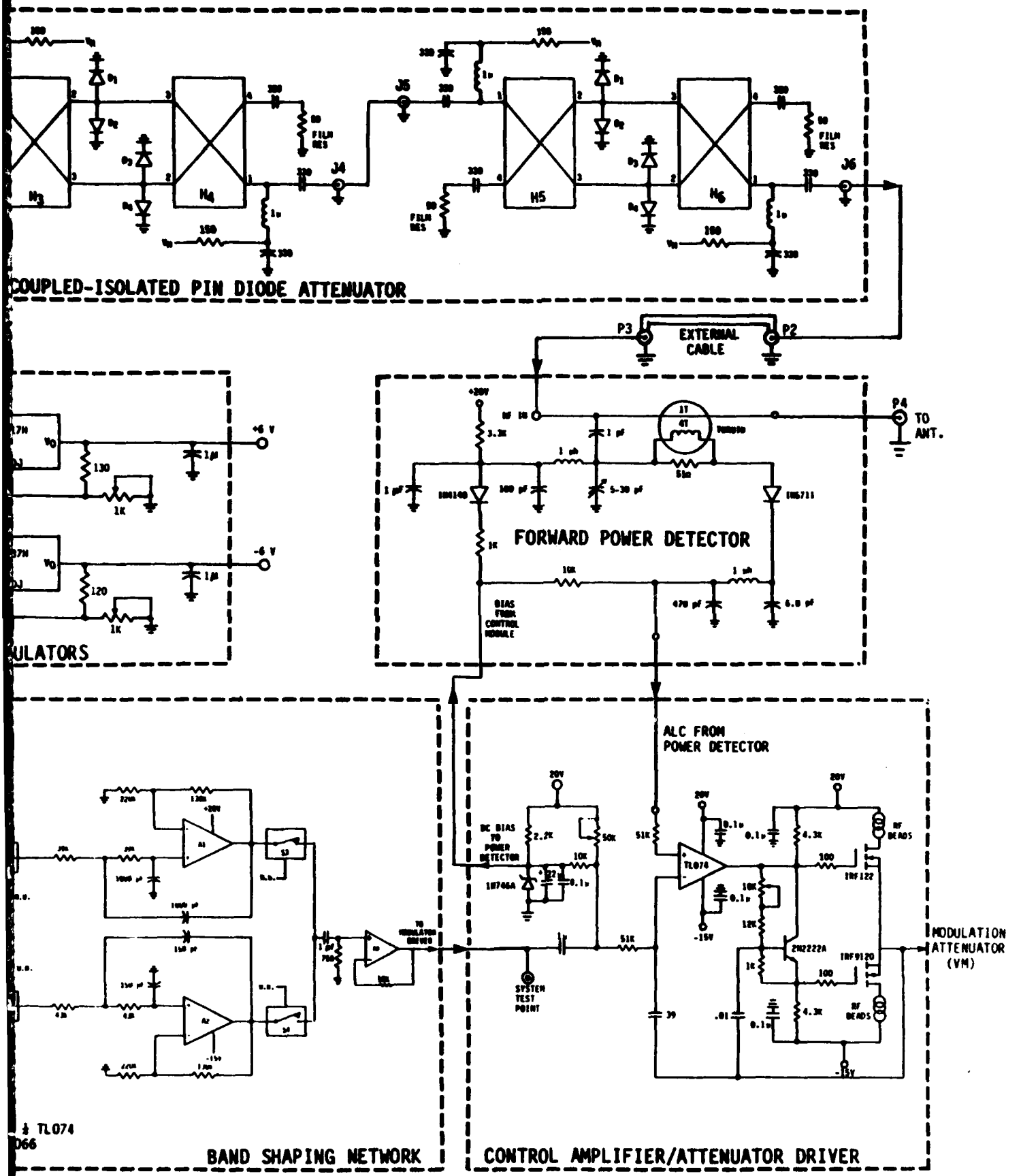


Figure 3.2-1. Modulator



Modulator Detailed Schematic

2

Paragraph 3.1.3 analyzes the degradation of the synthesiz noise performance caused by the noise figure of a loading device. Th synthesizer S/N degradation goal and requirement along with the required modulator noise figure is derived in paragraph 3.1.3 and sho in Table 3.2.1-1.

Table 3.2.1-1. N/S Degradation/dB

Buffer Amplifier Noise Figure/dB	$f_o \pm 10$ MHz
6	3
11	6

The maximum allowable synthesizer N/S degradation of 6 dI places a limit on the buffer amplifier's noise figure of 11 dB.

The buffer amplifier used in the deliverable, feasibilit; model was an Accrian UHF FET amplifier subassembly model PB4013. Amplitude and return loss for this packaged device is shown in Figur 3.2-1. The device's maximum gain of 18 dB is reduced by amplifier automatic level control (ALC); a dc voltage applied to the FET gate. The required 8 dB amplifier gain was achieved by fixing the ALC bias 10 volts. The measured amplifier noise figure is 11 dB. The worst case measured input VSWR occurs at 225 MHz as shown in Figure 3.2.1- where an input return loss of 11.5 dB is shown at this frequency. T VSWR is found by:

$$\text{VSWR} = \frac{\text{RL} + 1}{\text{RL} - 1}$$

where RL is the return loss. Hence RL = 14.13 (11.5 dB) and

$$\text{VSWR} = \frac{15.13}{13.13} = 1.15{:}1$$

The amplifier was case mounted to a convection cooled he sink which serves as the mechanical base for the modulator. Long te operation of the amplifier showed no appreciable rise in case tem- perature for the approximately 30 watts of dc power dissipated in th buffer amplifier.

The amplifier input/output pins are mounted to a microst PC board which in turn is coupled to the modulator's input port and electronically controlled attenuator via coaxial cables.

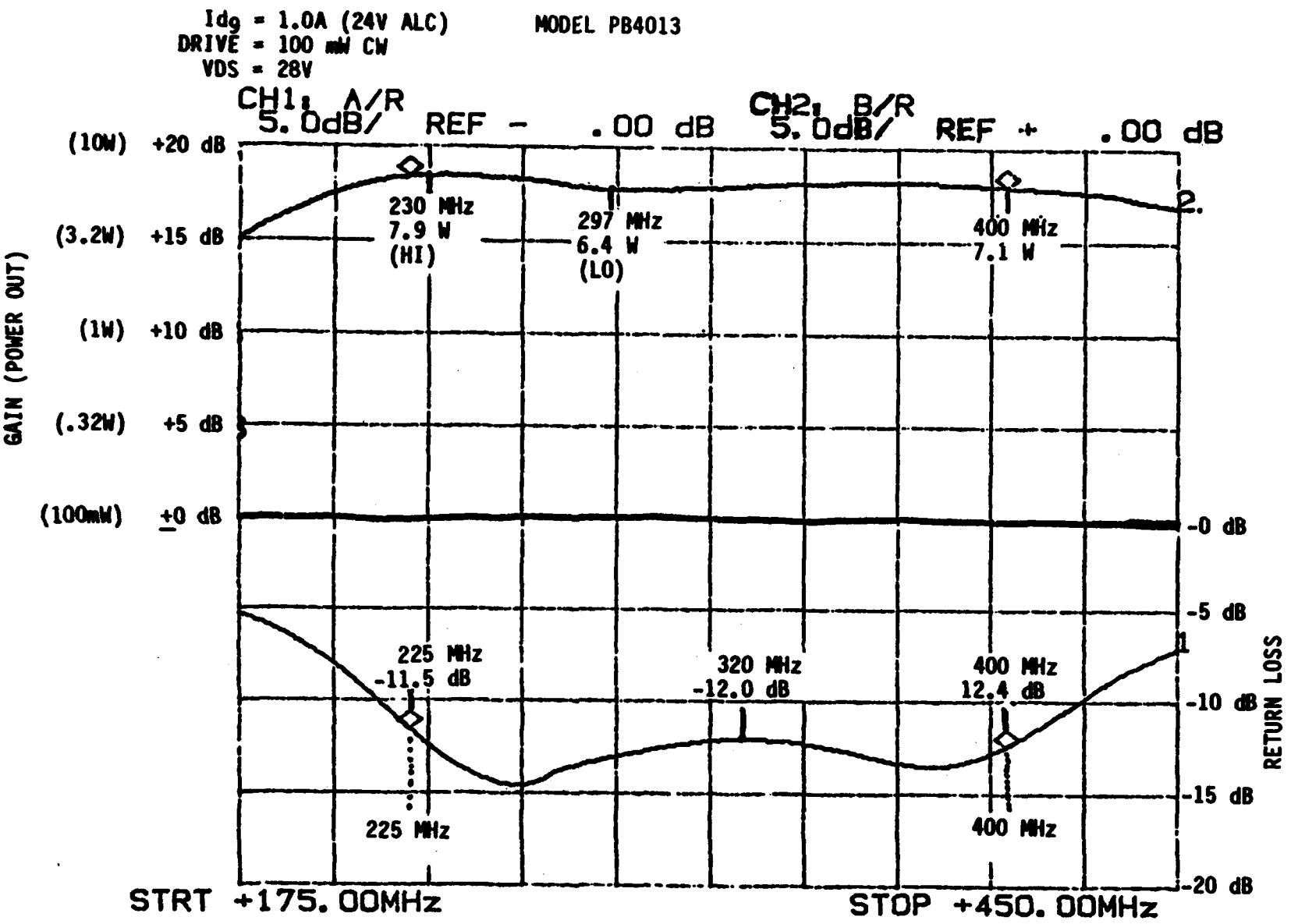


Figure 3.2.1-1. Buffer Amplifier Frequency Response

3.2.2 Electronically Controlled Pin Diode Attenuator

The requirements imposed on the pin diode attenuator were derived in paragraph 3.1.1 and are repeated in Table 3.2.2-1.

Table 3.2.2-1. Attenuator Characteristics

Modulation	Required Attenuation
Positive 85%	0 dB
Negative 90%	42 dB

The attenuator bias must provide for 8 dB of attenuation with no modulation. There is a decrease in attenuation during the positive modulation cycle swing and increasing attenuation during the negative modulation cycle excursion. The attenuator's input VSWR must be well controlled within the modulation cycle. A maximum attenuation of 50 dB (allows for system ALC and some margin) across the 225-400 MHz band requires careful attention to PC board layout and input/output isolation. Two attenuator models were constructed and tested during the breadboard phase. The design and test results of these models are discussed in paragraphs 3.2.2.1 and 3.2.2.2.

3.2.2.1 Controlled PIN Diode Attenuator

The variable attenuator must provide up to 50 dB attenuation of the 38 dBm (nominal) signal from the buffer amplifier. The input impedance of the attenuator is controlled to reduce the IFM that would result from a varying load on the synthesizer. A schematic of this circuit is shown in Figure 3.2.2.1-1. The circuit is made up of two cascaded bridged-T attenuators. The bridged-T configuration was chosen for this design because the modulation and impedance can be controlled separately by the shunt and series diodes, respectively.

In a 50 Ω system, the impedance requirements for the shunt and series diodes of the bridged-T attenuator are:

$$R_p(\Omega) = 50/\ (10^{(\alpha/20)} - 1) \qquad (11)$$

$$R_s(\Omega) = 50\ \ (10^{(\alpha/20)} - 1) \qquad (12)$$

where

R_p = shunt diode impedance
R_s = series diode impedance
α = attenuation in dB per stage

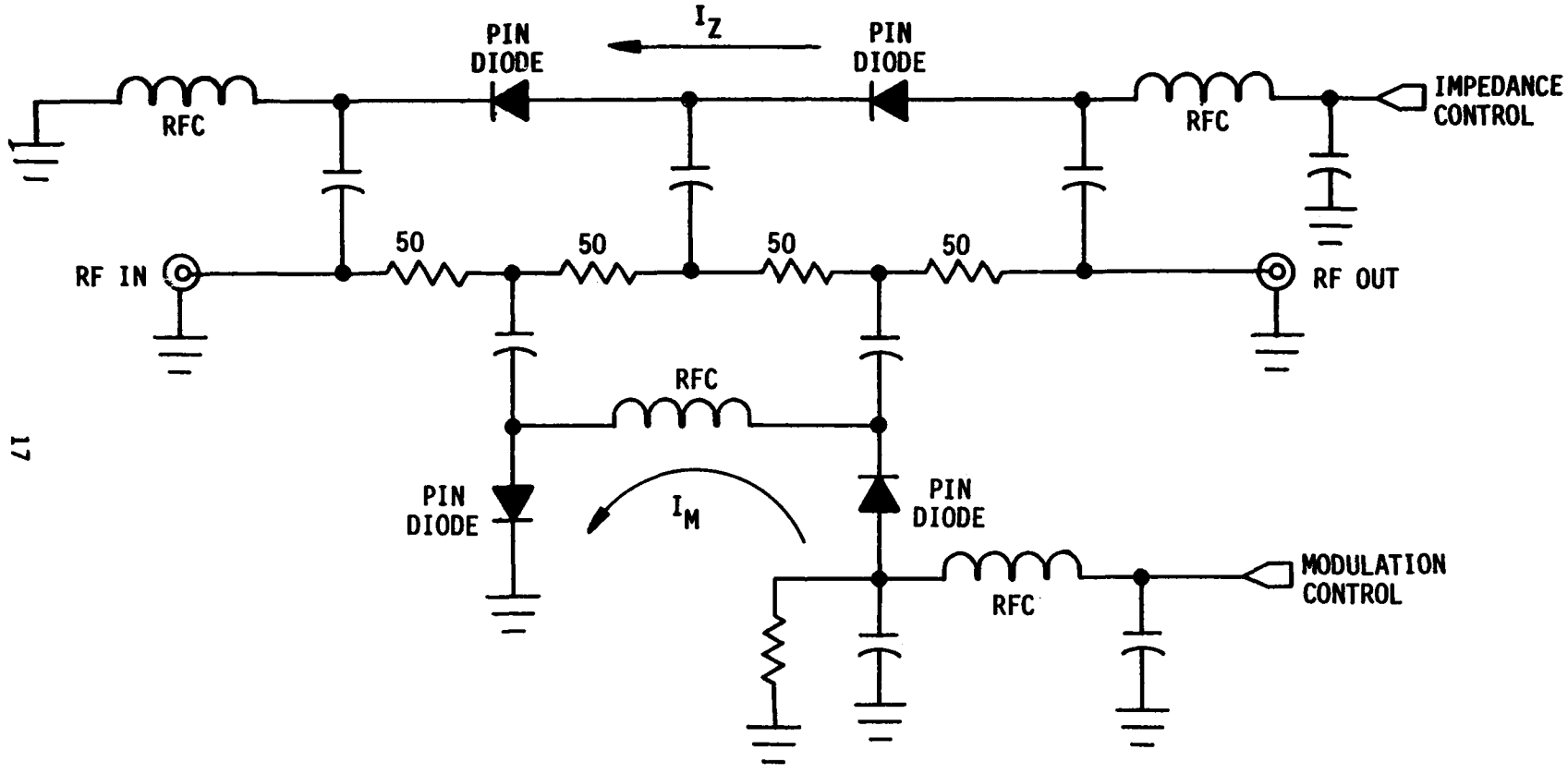


Figure 3.2.2.1-1. Controlled Pin Diode Attenuator

The system must provide two control loops for the PIN diode attenuator. The first control loop varies the current through the shunt diodes as a function of the modulation and the ALC signals. The second control loop varies the current through the series diodes as a function of the impedance detector signals.

The modulation bandwidth requires that the shunt diodes in the modulator loop operate at frequencies up to 25 KHz. The impedance loop tracks the modulation and therefore, the series diodes must operate at least a factor of ten higher in frequency, or up to 250 kHz. At these frequencies, the effect of minority carrier lifetime must be considered. The minority carrier lifetime must be significantly shorter than the period of the highest control signal frequency and significantly longer than the period of the lowest RF frequency. The requirements for the shunt and series diodes are as follows:

A) Shunt diode requires a minority carrier lifetime shorter than 1/25 KHz or 40 microseconds and longer than 1/225 MHz or 4.4 nanoseconds.

B) Series diodes require a minority carrier lifetime shorter than 1/250 KHz or 4.0 microseconds and longer than 1/225 MHz or 4.4 nanoseconds.

This shows that the requirements for the series diodes are the most demanding. The minority carrier lifetime for the series diodes should be around 400 nanoseconds.

The PIN diode attenuator of Figure 3.2.2.1-1 was carefully fabricated and tested. The circuit was constructed on a di-clad laminated dielectric PC board (Keene Di-Clad 527) using microstrip construction techniques. The 50 ohm resistors used were of thin film berillia ceramic (pyrofilm 300-10-3) construction. The PIN diodes shown in the figure were PILL packages (HP5082-3340) mounted in a shunt configuration for microstrip PC board construction. The bypass capacitors (330 pF) were standard chip capacitors also intended for microstrip installation.

Table 3.2.2.1-1 lists the test results taken from a network analyzer. The control levels (simulating modulation and impedance loops) were dc voltages.

Table 3.2.2.1-1. PIN Diode Attenuator Characteristics

Frequency (MHz)	Attenuation (dB)	Input VSWR	Control Level (Vdc)
225	2.1	2.6	0
225	10.2	2.1	4.46
225	22.1	1.5	5.94
225	28.6	1.3	6.31
225	52.4	1.12	10
400	2.3	2.43	0
400	9.6	1.98	4.46
400	20.1	1.43	5.94
400	25.3	1.23	6.31
400	39.6	1.06	10

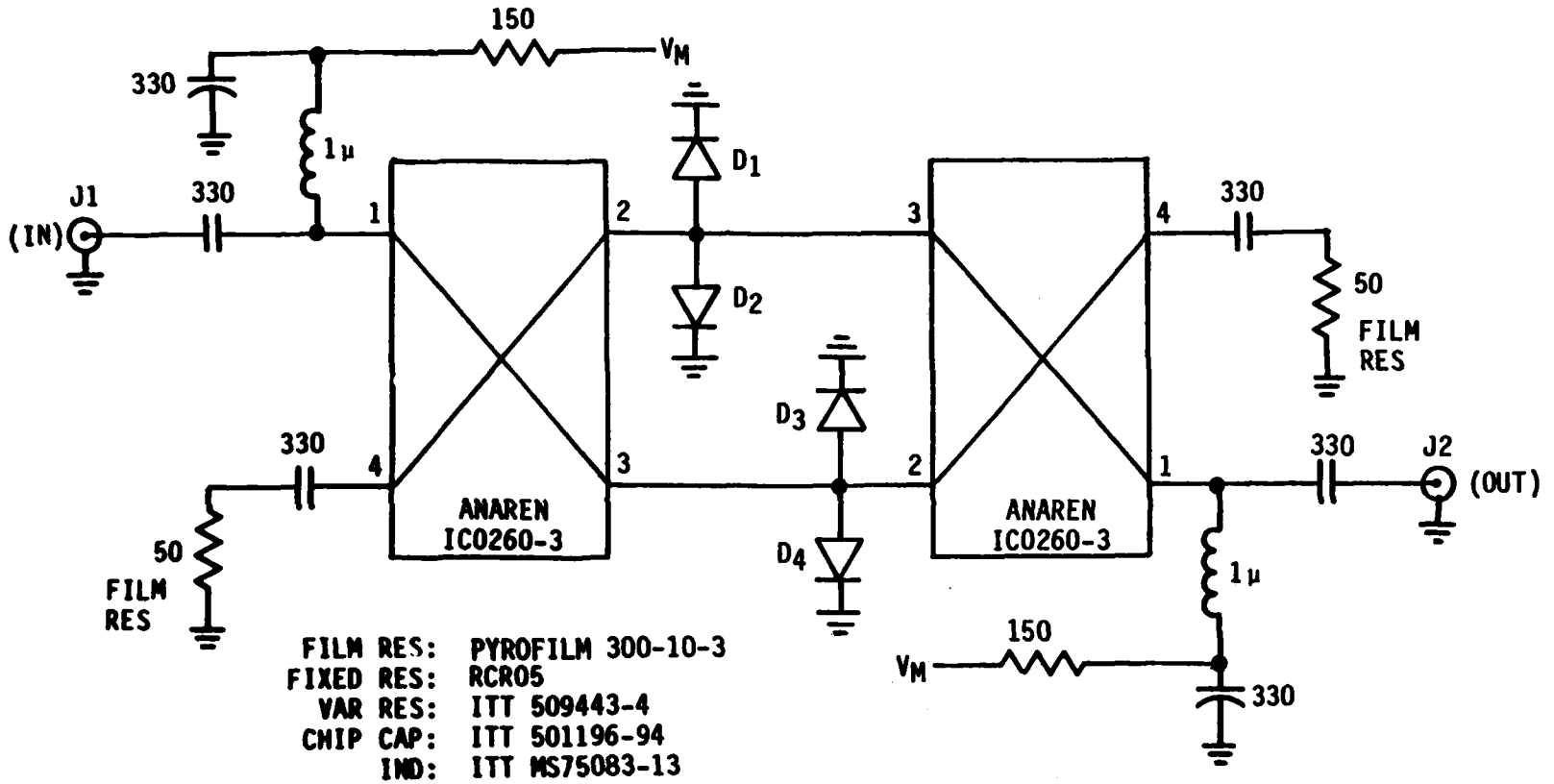
The tabulated results show a marginal attenuation level at the 400 MHz frequency while the VSWR at the low frequency end of the band was greater than required (VSWR $\leq$2.1).

A subsequent investigation showed the degraded VSWR stemmed from approximately 1.5 pF of stray capacitance across the 50 ohm power resistors. Modeling the circuit on COMPACT and inserting the resistor's stray capacity into the computer program simulation circuit confirmed the results of Table 3.2.2.1-1.

3.2.2.2 Hybrid Coupled-Isolated PIN Diode Attenuator

Figure 3.2.2.2-1 is a detailed schematic of one stage of a three stage hybrid coupled-isolated PIN diode attenuator. The purpose of the hybrid coupler is to isolate the input port (No. 1) from the output ports (Nos. 2 and 3). Port No. 4 is terminated in the coupler's characteristic impedance and absorbs any power mismatch introduced by the loads at ports 2 and 3. The impedance variations of the PIN diodes and the stray capacity of the 50 ohm power resistor (discussed in paragraph 3.2.2.1) are isolated from the input port resulting in an excellent attenuator input VSWR across the frequency band.

A desirable characteristic of the hybrid attenuator is the isolation of the PIN diode impedance variation from the source. This permits control of the diodes in only one control loop (ALC) instead of the two loops (impedance and ALC). The dc bias for the PIN diodes is fed into the input port (No. 1) permiting the diodes to terminate the output ports (Nos. 2 and 3) directly rather than through a dc blocking capacitor. The breadboard and subsequent feasibility model used an ANAREN (ICO 260-3) 90 degree-hybrid coupler.



FILM RES: PYROFILM 300-10-3
FIXED RES: RCR05
VAR RES: ITT 509443-4
CHIP CAP: ITT 501196-94
IND: ITT MS75083-13
DIODE: UM6201B
RECEP: NANOHEX (SEALECTRO) 51-453-0000
HYBRID: ANAREN IC0260-3

Figure 3.2.2.2-1. 1-Stage of a 3-Stage Hybrid Coupled-Isolated Pin Diode Attenuator

A three stage attenuator, shown in Figure 3.2-1, was constructed. The attenuation and reflection coefficient of the three stage attenuator as a function of frequency are shown in Figure 3.2.2.2-2. This network analyzer plot shows the attenuation (S21) across the 225-400 MHz band to range from -0.9 dB to -1.5 dB for zero volt modulation level while the maximum attenuation shows a range of -65 to -62 dB at the same frequencies for a 2 Vdc input level (V_M in Figure 3.2.2.2-1). A constant attenuation level across the frequency band is not critical to modulator performance due to error correction by the system ALC. The minimum and maximum attenuation of 1.5 dB and 62 dB respectively are more than adequate for the modulator's percentage modulation requirements.

The input VSWR across the band is calculated, as before, from the input reflection coefficient. The worst case input VSWR calculated from a 12 dB reflection coefficient (S11) at 360 MHz is then 1.13:1.

The attenuation as a function of drive (modulation) voltage of the 3 stage attenuator is plotted in Figure 3.2.2.2-3. It has good linearity over the 2 to 40 dB attenuation range.

Construction of the attenuator, as discussed previously, is critical. Figure 3.2.2.2-4 is a drawing of the 3-stage attenuator showing isolation (aluminum plates) between PIN diodes (D1/D2 and D3/D4 in Figure 3.2.2.2-1) and also between the 3 stages. The nano-hex input/output connectors and miniature 50 ohm coaxial cable are used. The construction of the attenuator permits ease of installation via card guides mounted on the modulator's side walls (see mechanical considerations in paragraph 3.2.6).

3.2.3 Forward Power Detector

A power level detector provides information for the attenuator control circuit to adjust modulation depth and provide automatic level control (ALC).

Detectors sample the voltage and the current on a transmission line as shown in Figure 3.2.3-1. The voltage sample can be derived from either a resistive or capacitive voltage divider between the transmission line and ground. In the 225-400 MHz band, a capacitive divider is preferred because it is less susceptable to stray capacitance than a resistive divider. As long as the voltage sample output is not loaded, it has the same phase as the line voltage. The magnitude of the sample voltage is

$$V_1 = \frac{C_1}{C_1 + C_2} V_T, \text{ where } V_T \text{ is the line voltage.}$$

The current is sampled with a toroidal transformer as illustrated in Figure 3.2.3-2.

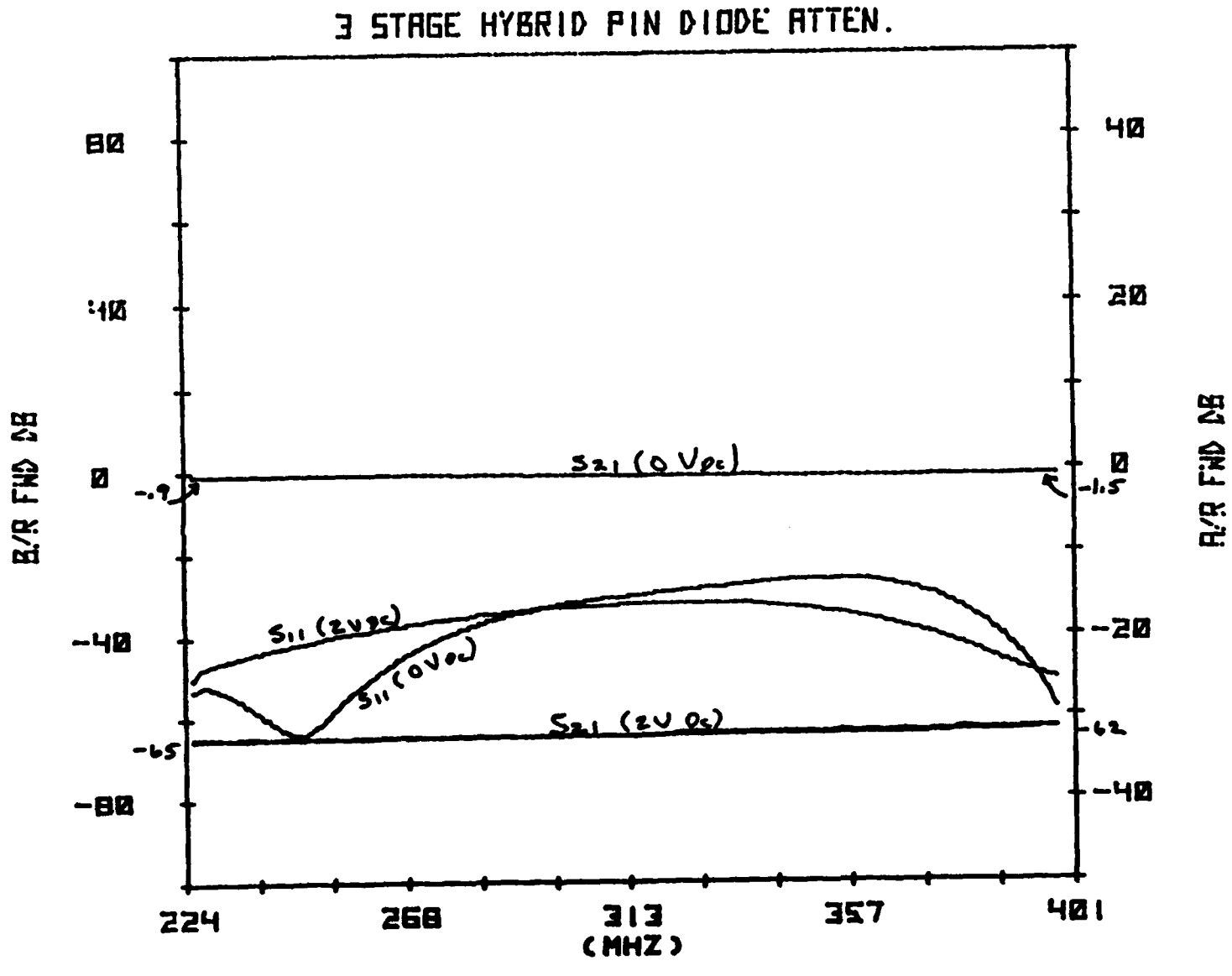


Figure 3.2.2.2-2. Hybrid Coupled, Pin Diode Attenuator Characteristics

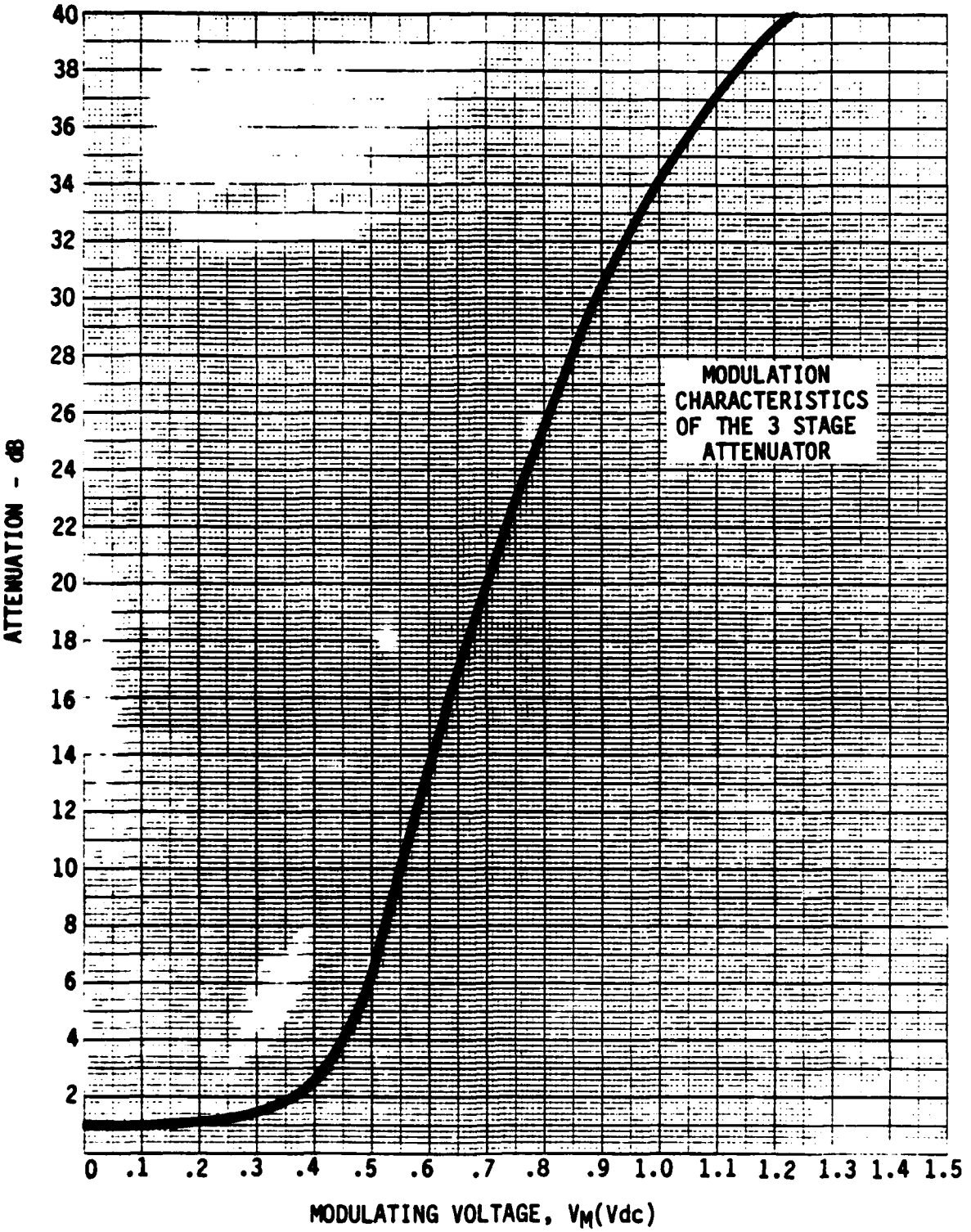


Figure 3.2.2.2-3. Attenuator Characteristic

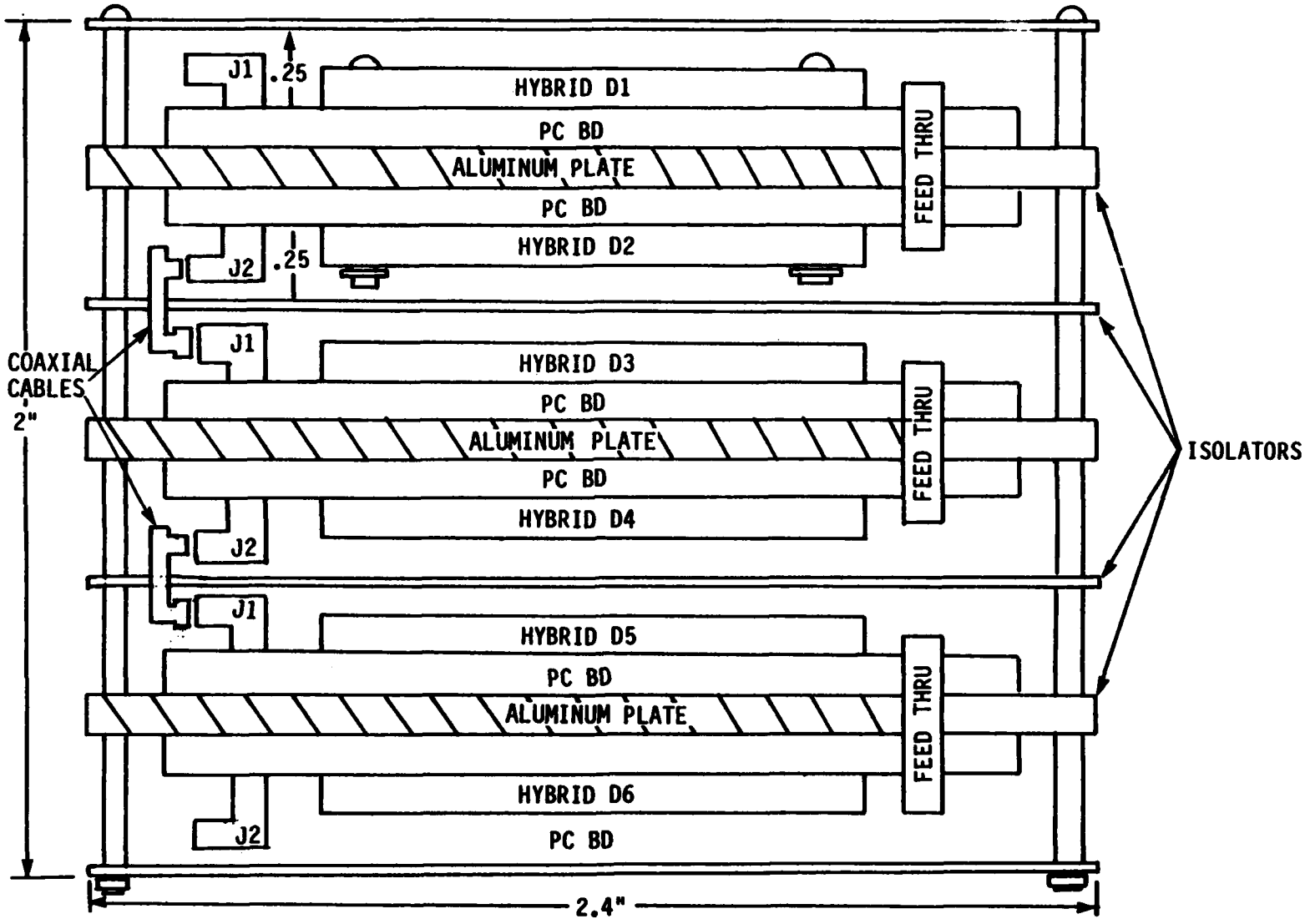


Figure 3.2.2.2-4. 3-Stage Hybrid Coupled Attenuator Construction

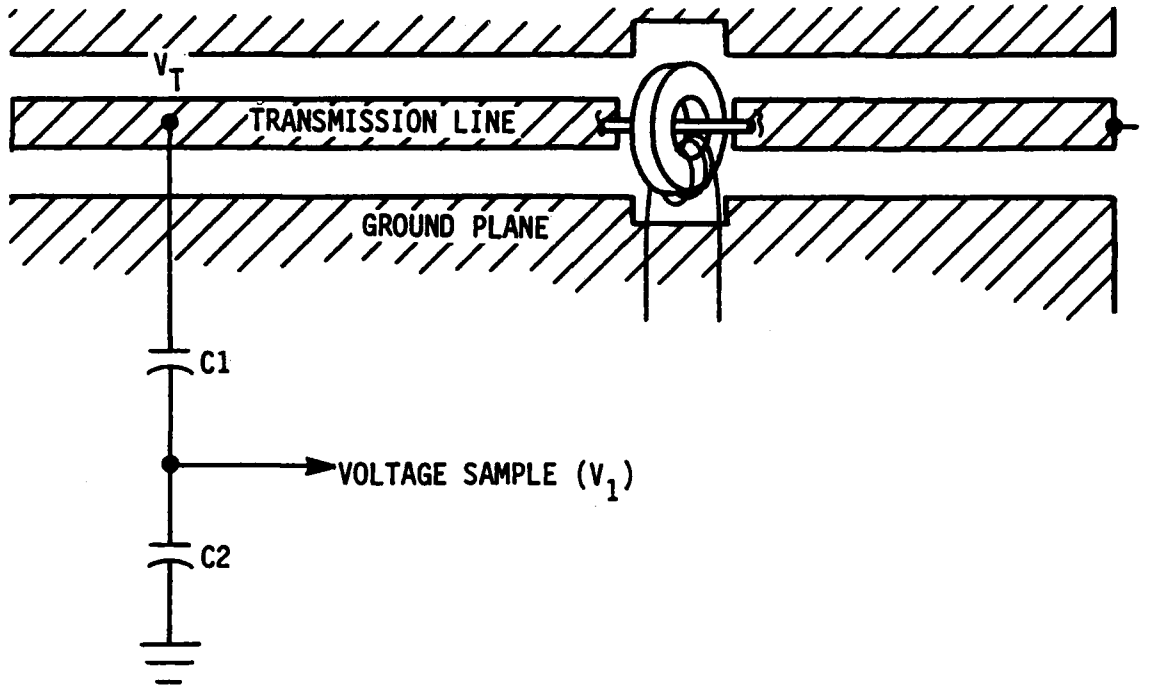


Figure 3.2.3-1. Voltage Sample

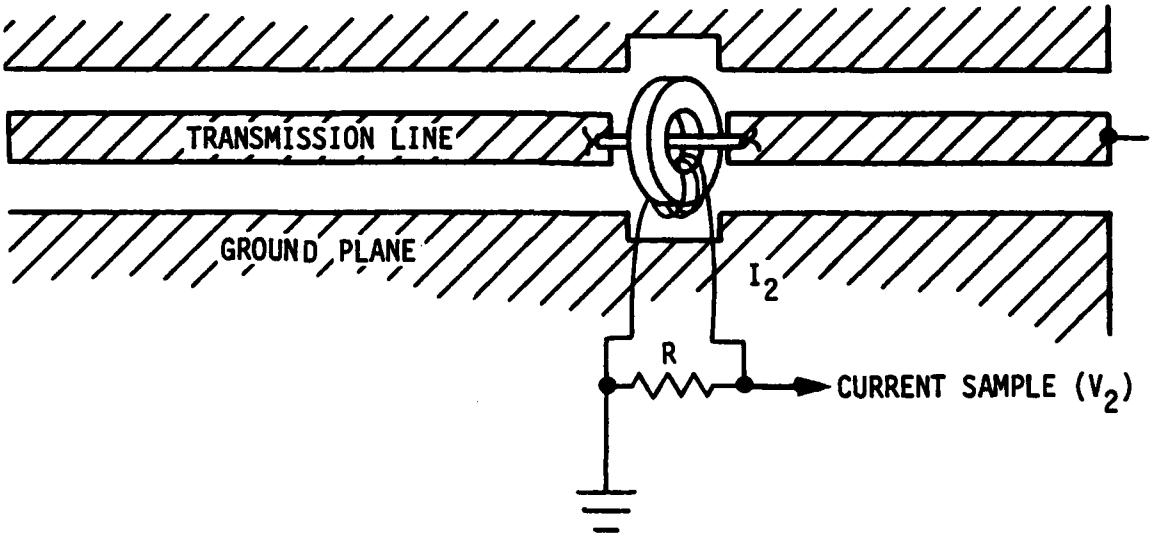


Figure 3.2.3-2. Current Sample

The current in the secondary winding is

$I_2 = I_T/N$, where I_2 is the secondary current, N is turns ratio, and I_T is the primary current.

When this current is loaded by a resistor, R, the voltage across this resistor is approximately

$$V_2 = I_2R = I_T(R/N)$$

V_2 is a voltage proportional to the current in the transmission line and in phase, or 180° out of phase, depending on the winding sense of the transformer. Figure 3.2.3-3 is a schematic of a completed forward power detector.

The operation of the forward power detector is straight forward. The voltage and current samples are equal when the impedance (Z) is 50 Ω. The two samples are added together as phasors at RF. The transformer is phased so that voltages add when driving 50 Ω. The output voltage is therefore proportional to the square root of the forward power on the line. The square root function is a result of the fact that the voltage and current samples are added and not multiplied. This is necessary to provide the modulation information to the control circuit that supplies the current to the attenuator's shunt diodes. The dc component of the detector output which is a measure of the carrier level provides an automatic level control (ALC) signal to the modulator.

The detector is located between the modulator and the 50 ohm load (antenna). The bias voltage is supplied by the control module to pre-bias the 1N5711 detector diode. The detected output which is sent to the control module consists of a dc level, corresponding to the RF carrier level, for system ALC and the audio modulation envelope to aid in maintaining low distortion in its modulated RF output signal.

Tests were conducted on the detector module with a 6 watt PEP RF input drive and a modulating frequency varying from 300 Hz to 25 kHz. The detected output level consisted of a 300 mV P-P audio envelope riding on an 800 mV dc voltage. The corresponding carrier distortion was less than 5 percent while the input VSWR was noted to be 1.03:1.

The foregoing test showed that performance of the detector was satisfactory.

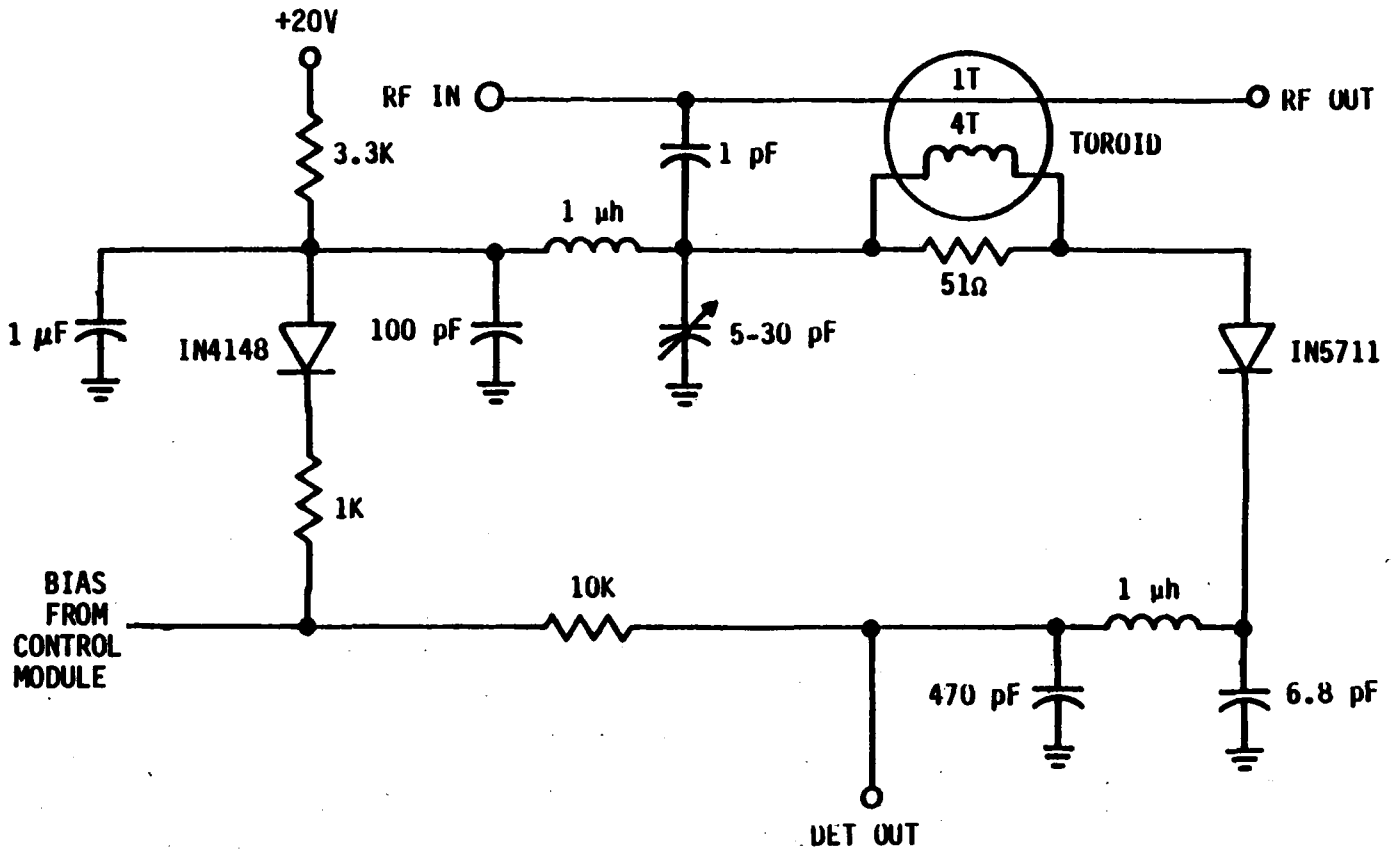


Figure 3.2.3-3. Forward Power Detector

3.2.4 Interface and Control Circuits

Requirements of the interface, band shaping, and control circuits are discussed in the following paragraphs.

3.2.4.1 Interface Module

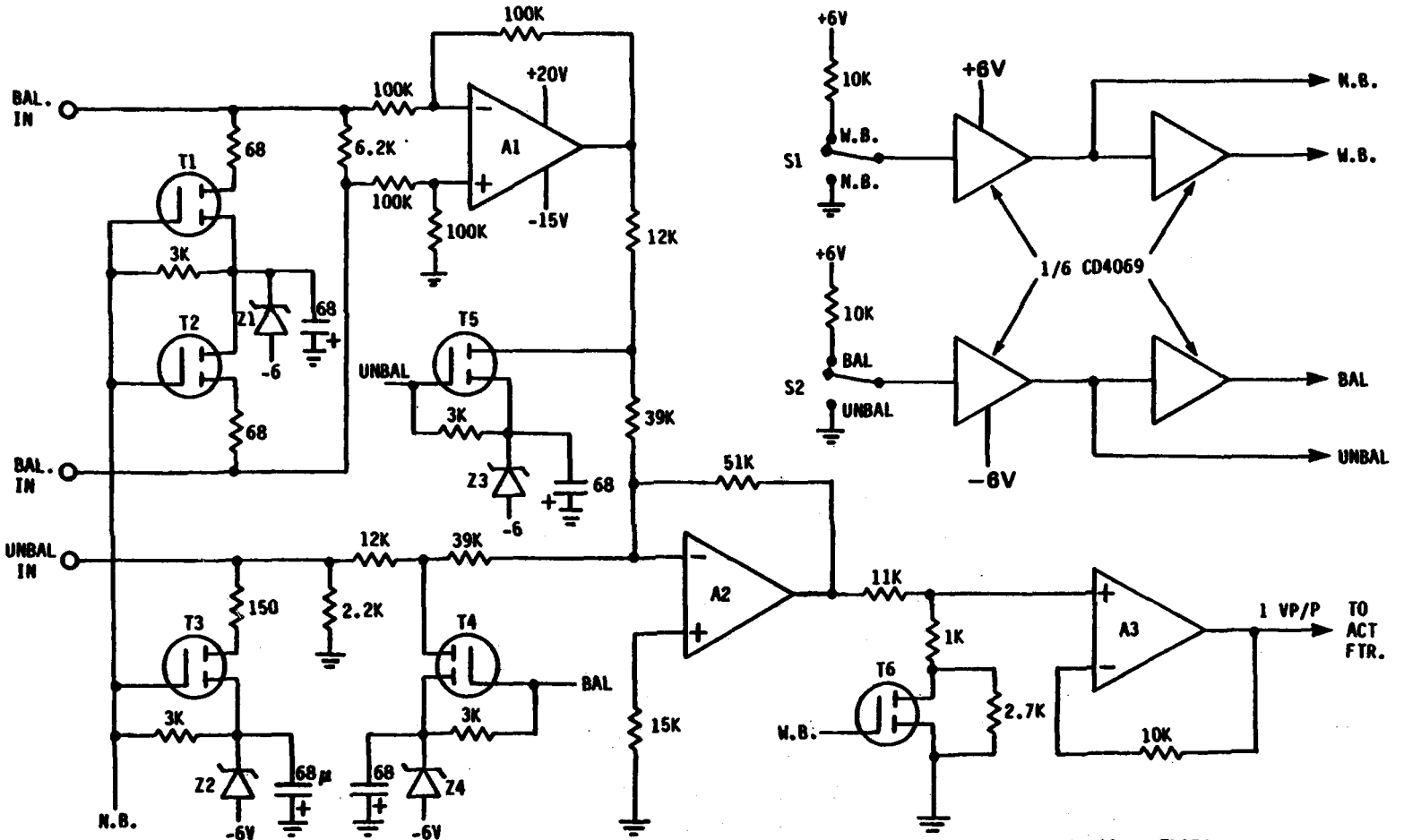
The interface module converts wide and narrowband modulating signals to a constant level for driving the control module. In addition to level control of the input signals the module provides both a balanced and an unbalanced input port, front panel mode selection switching, port input impedance control and output port isolation. These requirements are summarized in Table 3.2.4.1-1.

Table 3.2.4.1-1. Modulation Requirements

Parameter	Input Mode		Units
	Balanced	Unbalanced	
Input Impedance:			
Narrowband (300 to 3500 Hz)	150 $\pm$ 30	150 $\pm$ 30	Ohms
Wideband (300 to 2500 Hz)	6 $\pm$ 0.6	2 $\pm$ 0.2	K Ohms
Input Voltage:			
Narrowband	1.4	1.4	Vrms
Wideband	12	12	V p-p

The interface module converts the different input voltage levels (4 and 12V p-p) to a constant 1 volt p-p drive level to the control module to maintain a constant modulation percentage.

Figure 3.2.4.1-1 is a detailed schematic of the interface network module. The figure shows the balanced and unbalanced input ports terminated in the required input impedances (per table 3.2.4.1-1), via the T1/T2 and T3 FET stages, conversion of the balanced input port to an unbalance mode through amplifier A1, and combining both balanced and unbalanced modes in summing amplifier A2. FET T6 is enabled in the wideband operational mode to assure a constant modulating signal level output regardless of input mode. Amplifier A4 is an output buffer which provides a low impedance drive to the band shaping network. FET's T4 and T5 provide port isolation to the unused port. FET T6 is enabled by the selection of the unbalanced mode which grounds the output of A1, the balanced input port, thus isolating signals coupled into the modulator's balanced port. FET T4 is enabled in the balanced mode to produce similar results. Measurements show greater than 60 dB of input port isolation is obtained in this manner. A CD4069 integrated circuit provides the wideband/narowband gates to the switching FET stages (VN10LE). The operational modes (wideband/narrowband - balanced/unbalanced) are front panel controlled by panel mounted toggle switches. Zener diodes, Z1 through Z4, bias switching FET stages T1 through T5 to prevent high level modulation swings turning the FET stages to their on condition. Module testing showed:



		BAL	UNBAL	
Z_{IN} :	N.B.	150	150	(+20%)
	W.B.	6K	2K	(±10%)
E_{IN} :	N.B.	4VP/P		
	W.B.	12VP/P		

A1-A3 : TL074
T1-T6 : VN10LE
S1, S2 : MS24655-231
Z1-Z4 : 1N5995

Figure 3.2.4.1-1. Interface Network

- The input voltages are converted to a constant 1 V p-p output level.
- The input impedances are within tolerance.
- A port to port isolation of 60 dB.
- Signal balance is preserved at the balanced input.

3.2.4.2 Band Shaping Network

Figure 3.2.4.2-1 shows the band shaping network schematic. The module contains the 2 pole high pass and 2 pole low pass filters required to meet the band shaping requirements.

The high-pass filtering for a 300 Hz lower 3 dB frequency is provided by the input/output C-R (1 µf-750 ohm) networks. The low-pass filtering for either a 3500 Hz or a 25 kHz upper 3 dB cutoff frequency, is provided by active two-pole filters. Operational amplifier A1 is a 3500 Hz low pass filter while A2 is a 25 kHz low pass cutoff filter. Filter path gains are identical, thus preserving the modulating signal level. Switches S1 through S4 (CD4066 integrated circuit), controlled by the selected operational mode, choose the appropriate low pass filter. Module test results show:

- The cutoff frequencies to be within $\pm$5% of the required value shown in Table 3.2.4.1-1.
- The frequency roll-off is 9 dB per octave or greater at frequencies below the lower cutoff frequency (300 Hz) and above the upper cutoff frequencies (3.5 kHz and 25 kHz).
- Input signals of 6 V p-p can be tolerated at the input port. This results in a desirable margin for the nominal 1 V p-p input modulation level.

3.2.4.3 Modulation/ALC Control

Modulation and automatic level control in the EMC Enhanced Constant "Z" Modulator are provided in the same loop. A schematic of the control circuit for this loop is shown in Figure 3.2.4.3-1. The signal from the power detector is a voltage that is a function of the square root of the forward power. This voltage contains the modulation and a dc level representing the average power. This circuit can be analyzed by considering it to be a negative feedback linear amplifier. Applying the principle of superposition, the loop is set up with no modulation first to set the dc bias and then the modulation is applied and adjusted for the proper percent modulation.

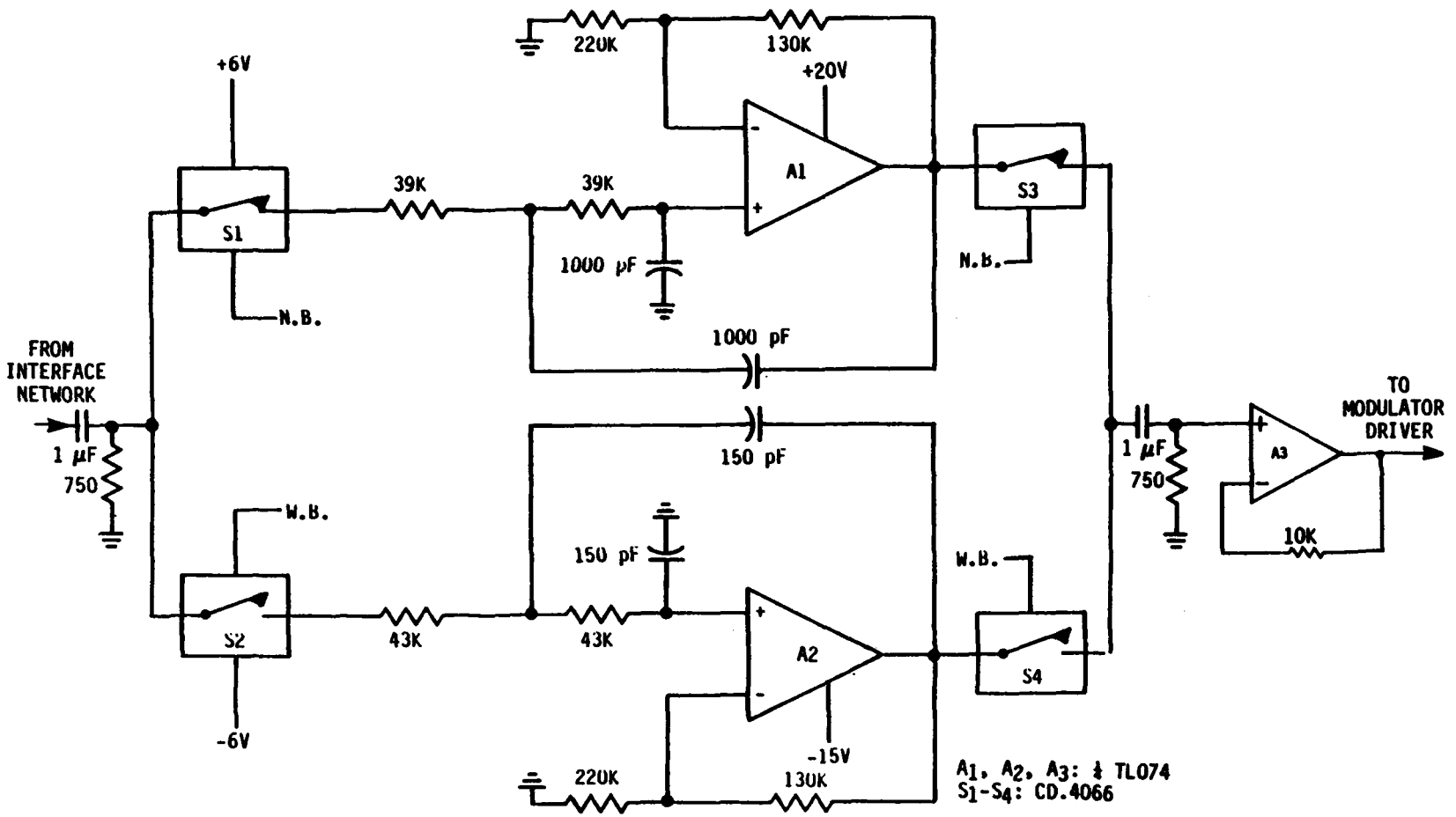


Figure 3.2.4.2-1. Band Shaping Network

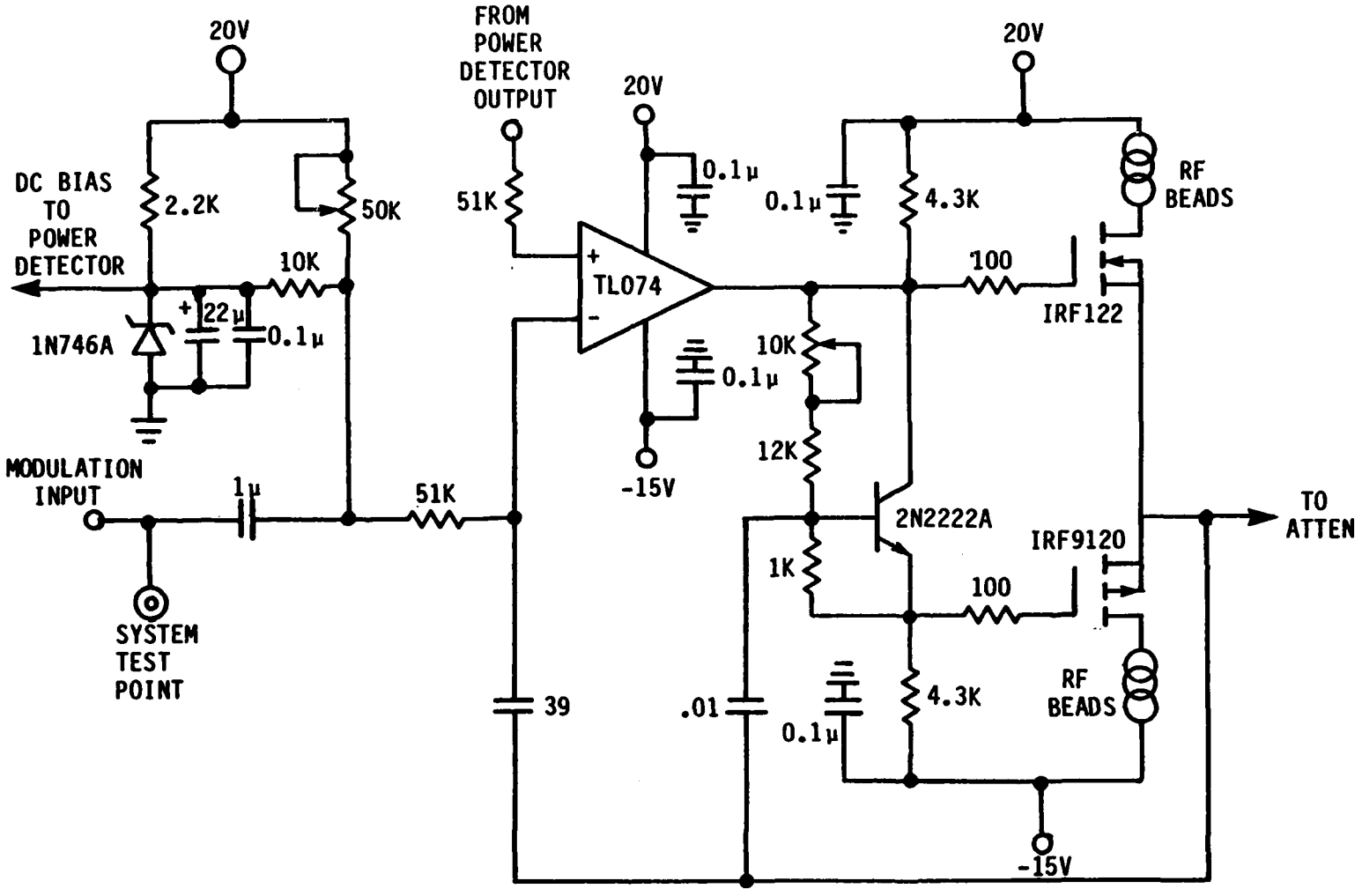


Figure 3.2.4.3-1. Control Amplifier/Attenuator Driver

The control module breadboard test results showed a frequency response of 230 kHz and a peak modulating input drive capability of 10 volts. The balanced FET drivers (IRF 122/9120) can reliably source and sink several amperes of drive current without heatsinks.

The >200 kHz frequency response is adequate to process the 25 kHz input modulating signals while the 1 volt peak modulating drive signals are well within the operational amplifiers (TL074) range. The 39 pF feedback capacitor enhances the drive linearity. A measured distortion of less than 0.5 percent for this stand-alone circuit is well within the modulator's overall distortion requirement.

The 50 kilohm potentiometer which is located on the front panel controls the ALC level. Provisions have been made for an optional power amplifier (see Figure 3.1-1) to be inserted between the attenuator and the power detector.

3.2.5 Mechanical Requirements

The constant Z modulator is self-contained in an aluminum housing mounted on an aluminum heatsink. Figure 3.2.5-1 is a picture of the complete modulator housing, the base heatsink, the input/output connectors and the front panel hardware.

Figure 3.2.5-2 is a detailed drawing of the assembled modulator showing the front panel assembly and the module locations. The amplifier is horizontally mounted to the modulator's base heatsink. Each module, except the RF amplifier, is card guide mounted for ease of maintenance. The front panel contains mode switches, the ALC control, and the modulation input ports. The RF connectors interface the modulator between the synthesizer (RF IN) and the antenna (RF OUT). The optional power amplifier (see Figure 3.1-1) would replace the cabling marked PA. The system test point (see Figure 3.2.4.3-1) permits examination of the modulating signal's characteristics such as amplitude, pass band and stop band parameters.

Operationally the packaged modulator showed the following:

- The amplifier heatsink was adequate to dissipate the 25-30 watts of dc power.

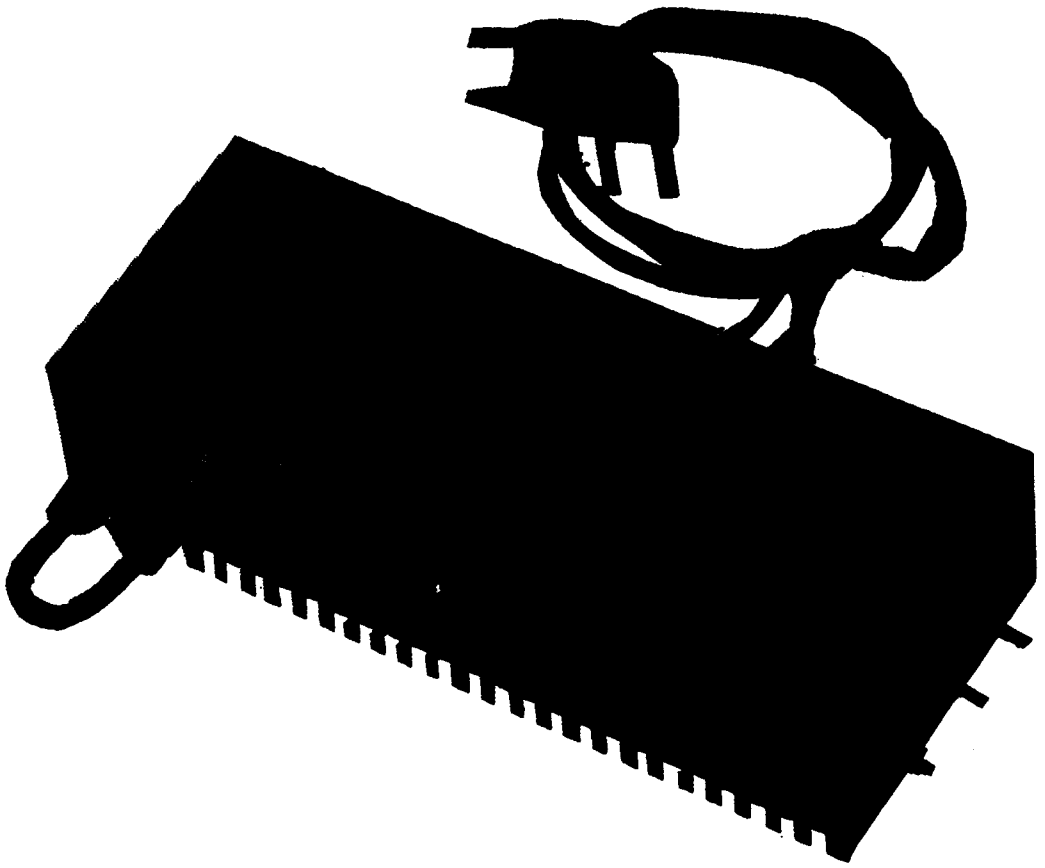


Figure 3.2.5-1. Modulator Enclosure

- The PIN diodes mounted in the first stage of the attenuator registered a high heat rise due to inadequate heatsinking. This stage attenuates the 6 watt carrier level prior to further attenuation by the succeeding stages. The heatsink for these glass diodes (unitrode 6200B) consists of a 1/8 inch aluminum plate connected to the aluminum sidewalls through the metal card guides. Modulator testing showed that the overheating PIN diodes resulted in increased PIN diode resistance which ultimately decreased the modulation percentage. The modulator's final tests were conducted utilizing a small bench fan cooling the housing's 'hot spot'.

- The RF isolation through the modulator was adequate as was the power supply bypasses.

3.2.6 System Testing

Breadboard system tests resulted in the replacement of the HP5082-3340 shunt mounted PIN diodes due to a carrer life time inadequacy. The typical carrier lifetime of 400 nanoseconds (HP data sheet parameter) was found to be deficient when the modulating frequency was greater than 10 kHz. A PIN diode with a typical carrier lifetime of 800 nanosecodns (UM6200B) was substituted for the HP device. This resulted in excellent dynamic results. The attenuator was retested on the network analyzer for swept frequency insertion loss and input VSWR as a function of modulating voltage. The measured results were similar to the responses of Figure 3.2.2.2-2 taken with the HP diodes.

System test results are discussed in Section 4 of this report.

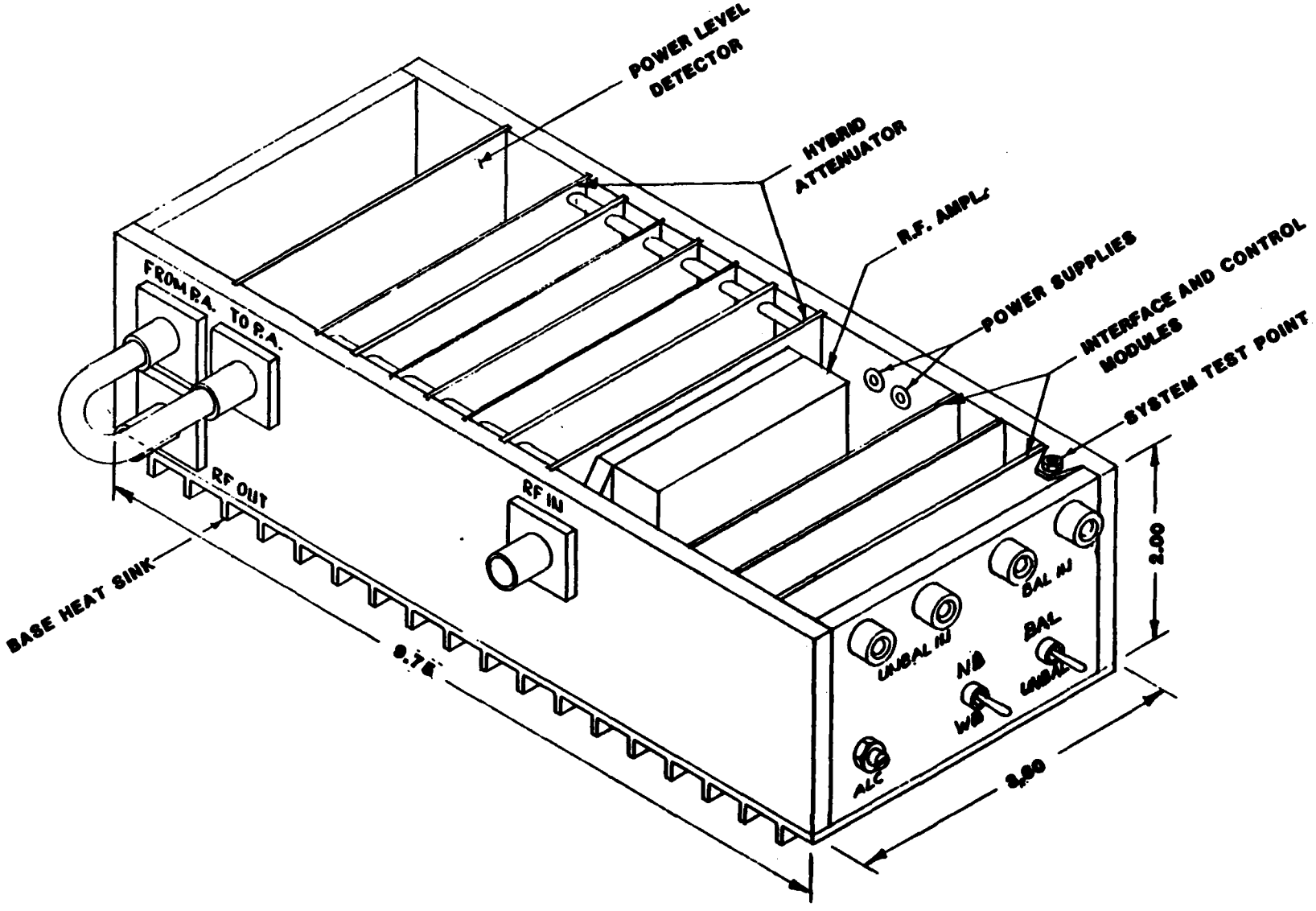


Figure 3.2.5-2. Modulator Package Concept

Section 4

SYSTEM TESTS

4.1 Modulator Test Results

System testing, including the final test, covered the system parameters shown earlier in Table 1.4-1. The final test results are given in Table 4.1-1 and each parameter is discussed in detail in this section.

4.1.1 Frequency Range

The specified 225 to 400 MHz frequency range requirement was easily met. The actual usuable range extends from 210 MHz to 450 MHz, being restricted on the low frequency band edge by the modulation distortion arising from the PIN diode minority carrier lifetime and on the high band edge by the buffer amplifier's frequency response.

4.1.2 Input Power

The input power handling capability exceeded the required 30-33 dBm range by a comfortable margin of $\pm$ 3 dB minimum. Testing over the frequency range showed the system ALC capable of maintaining the required modulation percentage over an input power as low as 0.25 watts (+24 dBm) to as large as 6 watts (+38 dBm). The input power level was not increased beyond the 6 watt limit due to possible buffer amplifier permanent degradation.

4.1.3 Input/Output Impedance

The modulator's nominal 50 ohm impedance level showed a VSWR of 1.4:1 maximum over the operating frequency range. The 1.4:1 VSWR represents a resistive impedance level of 35 or 70 ohms. The measurement was made with audio modulation. With a +85, -90 percent modulation at the modulator the measured incidental AM at the output of the synthesizer was 0.2%. This modulation isolation is necessary to prevent incidental frequency modulation of the synthesizer source drive.

4.1.4 Insertion Loss

The measured insertion loss was less than 2 dB.

Table 4.1-1. System Final Test Results

PARAMETER	SPECIFICATION	GOAL	FINAL TEST
Frequency Range	225 to 399.975 MHz		225-400 MHz
Input Power	30-33 dBm		30-33 dBm
Insertion Loss	<4 dB		1.8 dB Max.
Input Impedance	50Ω Nominal	VSWR ≤2:1	1.4:1 Max.
Output Impedance	50Ω Nominal	VSWR ≤2:1	1.4:1 Max.
Output Signal-to-Noise Degradation	≤6 dB	≤3 dB	6 dB Max.
Incidental FM	≤2.5 kHz		1.25 kHz Max.
Modulation Frequency (3 dB Bandwidth)			
Narrowband	300 Hz to 3.5 kHz	Nominal	290 Hz to 3.6 kHz
Wideband	300 Hz to 25 kHz	Nominal	317 Hz to 25 kHz
Minimum Modulation Capability			
Narrowband (1 kHz at 1.4 Vrms)	+85% - 90%		85% - 90%
Wideband (1 kHz at 12 V_{pp})	+85% - 90%		84.7% - 89.7%*
Distortion (90% Negative Modulation)	10%	5%	2.5% Max.
Modulation Input Impedance			
Narrowband			
Balanced	150Ω ± 20%		140 Ohms
Unbalanced	150Ω ± 20%		149 Ohms
Wideband			
Balanced	6000Ω ± 10%		6650 Ohms*
Unbalanced	2000Ω ± 10%		2180 Ohms

*Exceeded specifications

4.1.5 Output Signal-to-Noise (S/N) Degradation

The output S/N degradation was carried out by measuring the modulator's noise figure. Table 3.1.3-1 relates the device noise figure to the synthesizer S/N degradation parameter while paragraph 3.1.3 derives the mathematics for the table.

The modulator's noise figure, measured at 246, 312, and 360 MHz, ranges from 10.8 to 11 dB. The calculated S/N degradation was shown to be $\leq$6 dB at the measured low, mid, and high band frequency ranges.

4.1.6 Incidental FM (IFM)

The incidental FM requirement of $\leq$2.5 kHz was demonstrated by monitoring the modulated carrier with the modulator driven by the low noise synthesizer. The measured frequency deviation of 1.25 kHz maximum resulted from responses taken at 10 MHz increments over the synthesizers 225-400 MHz frequency range. The 1.25 kHz represents a 0.0003 percent induced frequency error in the synthesizer's selected frequency.

4.1.7 Modulation Bandwidth

The nominal 300 to 3500 Hz narrowband and 300 to 2500 Hz wideband bandwidth requirements were slightly exceeded as shown in the table. These non-critical responses are governed by the low and high pass filter sections located on the band shaping module. Judicious component selection (or variable resistors) would be necessary to meet the exact frequency responses as stated.

In addition the SOW also required stopband responses of 6 dB/octave minimum outside the nominal pass bands shown in Table 4.1-1. Measured stop band results taken at octave increments above and below the pass bands show a $\geq$8 dB roll off characteristic.

4.1.8 Modulation Capability

The +85%, -90% minimum modulation capabilty at the narrow and wideband voltage levels shown were met in the narrowband modulation mode but were 0.3% under the minimum in the wideband mode.

This deficiency is easily corrected by initiation of the front panel ALC control. During the final tests the under-modulation condition was found to exist during the exercise of the wideband-balanced input modulation mode; thus correcting the level by the ALC potentiometer adjustment would influence the previous modulation mode test results and this corrective action was not taken.

4.1.9 Distortion

Measured distortion levels of the modulated RF carrier (1 kHz modulation) showing 2.5 percent maximum over the RF frequency band were well under the 5% goal, 10% max criteria. This parameter is linked to the carrier's modulation percentage and modulator insertion loss. Care must be taken in the set-up of the ALC control to prevent an over modulation condition derived from large (>15 V p-p) input modulating signals.

4.1.10 Modulation Input Impedance

The modulation input impedances at the narrow and wideband ports were met except in the wideband-balanced operational mode.

These non-critical parameters are set by the input shunt resistors loading the input ports. Careful selection of the 6.2K ohm resistor in the balanced input port (see Figure 3.2.4.1-1) would be required to meet the 6000 ohm nominal input impedance.

4.2 Test Data Summary

The measured data of Table 4.1-1 shows most of the test requirements being met. In the case of the critical parameters (input power, insertion loss, IFM, S/N degradation, distortion, and modulation capability) only the modulation requirements of the wideband-balanced mode were compromised and then only by 0.3%. All non-critical parameters except the wideband-balanced modulation input impedance were met. As discussed in paragraph 4.1.11 action could be taken to guarantee the impedance to be within specification as well.

In summary, the final testing of the modulator resulted in excellent correlation with the program's stated goals and specifications.

Section 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

The program goal of the EMC Enhanced Constant "Z" Modulator was the development of an amplitude modulator operating in the UHF region as a companion modulation scheme for a low phase noise frequency hopping synthesizer presently under development at ITT-A/OD.

The 12 month RADC sponsored program encompassed research, breadboard and feasibility model stages that resulted in accomplishment of the SOW goals and specifications. The program drew upon results from a previous ITT-A/OD sponsored IR&D program investigating the amplitude modulation scheme eventually employed in the EECZM.

5.2 Recommendations

Recommendations for a modulator follow-on study include:

- Repackaging of the electronic attenuator to eliminate the input stage PIN diode 'hot spot'. This task could be accomplished by testing various 'shunt' type diodes similar in configuration to the HP5082-3340 microstrip power switching diodes or by designing a more optimum heatsink configuration for the presently used Unitrode UM6200B diodes.

- Further development of a low noise figure input buffer amplifier to reduce the synthesizer S/N degradation to meet the 3 dB goal.

- Conduct environment testing on the modulator in areas of vibration, shock, temperature and altitude to determine compliance with MIL-standard requirements.

Section 6

APPENDIX

This section includes the following vendor data sheets.

- Unitrode UM6200B PIN diode.
- Hewlett Packard HP5082-3340 microstrip PIN diode.
- ANAREN IC0260-3 3 dB, 90° hybrid coupler.

PIN DIODE

UM6000 SERIES
UM6200 SERIES
UM6600 SERIES

Features

- Capacitance specified as low as 0.4 pF (UM6600)
- Resistance specified as low as 0.4Ω (UM6200)
- Voltage ratings to 1000V
- Power dissipation to 6W

Description

These series of PIN diodes are designed for applications requiring small package size and moderate average power handling capability. The low capacitance of the UM6000 and UM6600 allows them to be used as series switching elements to 1 GHz. The low resistance of the UM6200 is useful in applications where forward bias current must be minimized.

Because of its thick I-region width and long lifetime the UM6000 and UM6600 have been used in distortion sensitive and high peak power applications, including receiver protectors, TACAN, and IFF equipment. Their low capacitance allows them to be useful as attenuator diodes at frequencies greater than 1 GHz. The UM6200 has been used successfully in switches in which low insertion loss at low bias current is required.

The "A" style package for this series is the smallest Unitrode PIN diode package. It has been used successfully in many microwave applications using coaxial, microstrip, and stripline techniques at frequencies beyond X-Band. The "B" and "E" style, leaded packages offer the highest available power dissipation for a package this small. They have been used extensively as series switch elements in microstrip circuits. The "C" style package duplicates the physical outline available in conventional ceramic-metal packages but incorporates the many reliability advantages of the Unitrode construction.

MAXIMUM RATINGS

Average Power Dissipation and Thermal Resistance Ratings

Package	Condition	UM6000 UM6200		UM6600	
		P_D	θ	P_D	θ
A&C	25 °C Pin Temperature	6W	25 °C/W	4W	37.5 °C/W
B&E (Axial Leads)	½ in. Total Lead Length to (12.7 mm) to 25 °C Contact	2.5W	60 °C/W	2.0W	75 °C/W
B&E (Axial Leads)	Free Air	0.5W	—	0.5W	—

Peak Power Dissipation Rating

All Packages	1 μs Pulse (Single) at 25 °C Ambient	UM6000 - 25 KW UM6200 - 10 KW	UM6600 - 13 KW

Operating and Storage Temperature Range: −65 °C to +175 °C

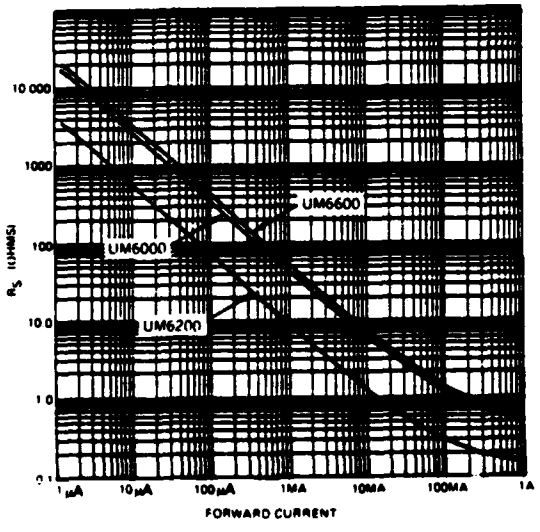
Voltage Ratings (25 °C)

Reverse Voltage (V_R) — Volts (I_R = 10 μA)	Types		
100V	UM6001	UM6201	UM6601
200V	UM6002	UM6202	UM6602
400V	—	UM6204	—
600V	UM6006	—	UM6606
1000V	UM6010	—	UM6610

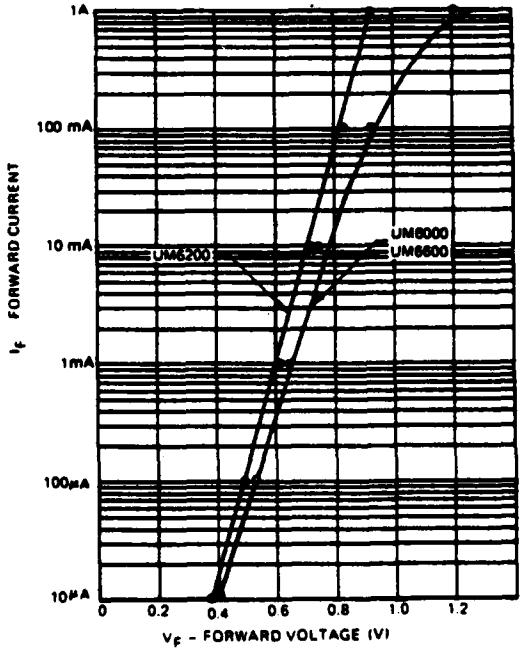
Electrical Specifications (25 °C)

Test	Symbol	UM6600	UM6000	UM6200	Conditions
Total Capacitance (Max)	C_T	0.4 pF	0.5 pF	1.1 pF	0V, 1 GHz
Series Resistance (Max)	R_S	2.5Ω	1.7Ω	0.4Ω	100 mA, 1 GHz
Parallel Resistance (Min)	R_P	10 KΩ	15 KΩ	10 KΩ	100V, 1 GHz
Carrier Lifetime (Min)	τ	1.0 μs	1.0 μs	0.6 μs	I_F = 10 mA
Reverse Current (Max)	I_R	10 μA	10 μA	10 μA	V_R = Rating
I-Region Width (Min)	W	150 μm	150 μm	40 μm	—

TYPICAL SERIES RESISTANCE
VS
FORWARD CURRENT
(F = 100MHz)



DC CHARACTERISTICS
FORWARD VOLTAGE VS CURRENT



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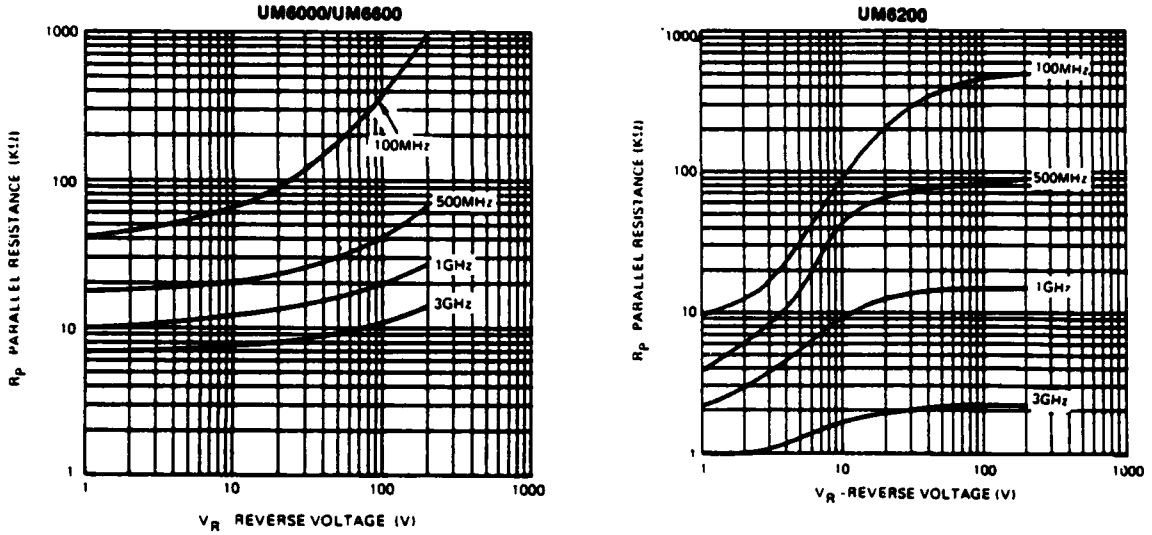
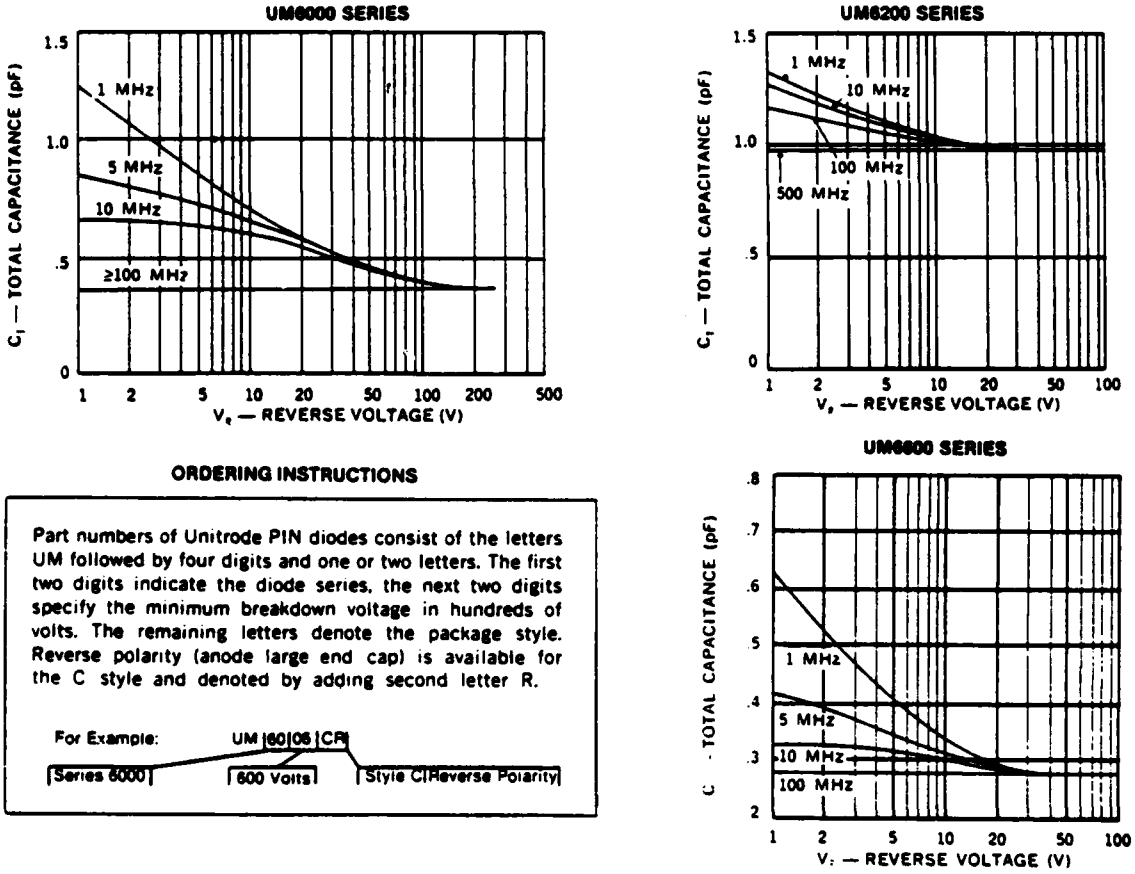
TYPICAL R_p VS VOLTAGE & FREQUENCY



TYPICAL CAPACITANCE VS VOLTAGE AND FREQUENCY



ORDERING INSTRUCTIONS

Part numbers of Unitrode PIN diodes consist of the letters UM followed by four digits and one or two letters. The first two digits indicate the diode series, the next two digits specify the minimum breakdown voltage in hundreds of volts. The remaining letters denote the package style. Reverse polarity (anode large end cap) is available for the C style and denoted by adding second letter R.

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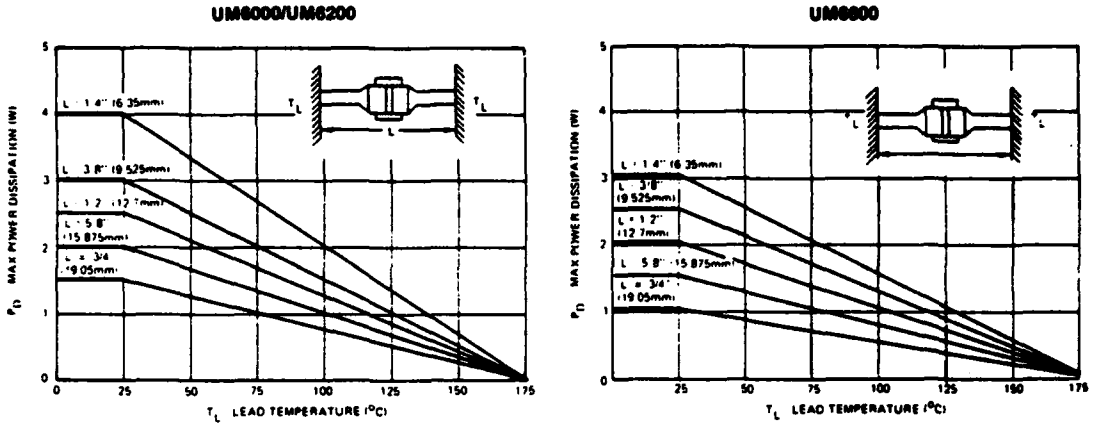
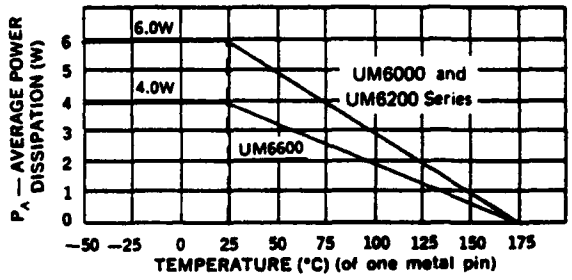
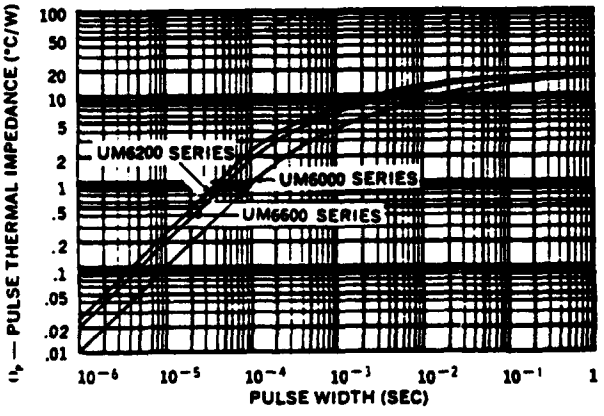
POWER RATING — AXIAL LEADED DIODE



POWER RATING



PULSE THERMAL IMPEDANCE VS PULSE WIDTH



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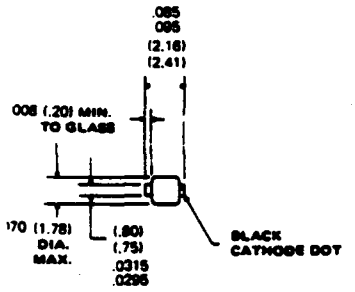
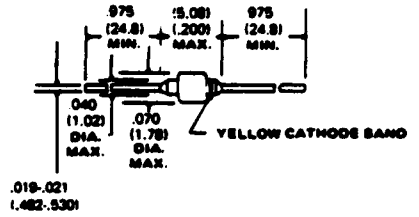
MECHANICAL SPECIFICATIONS

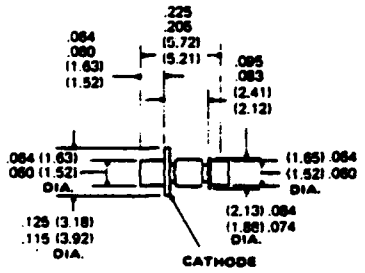
STYLE A



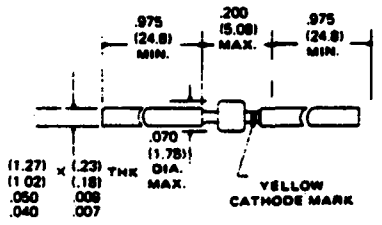
STYLE B



STYLE C
CARTRIDGE



STYLE E
RIBBON LEADS



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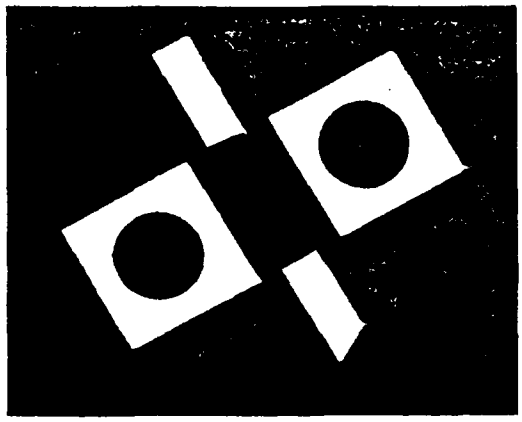
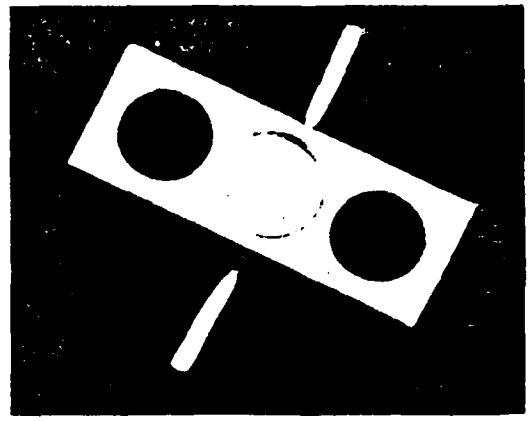
HEWLETT PACKARD

PIN DIODES FOR STRIPLINE AND MICROSTRIP SWITCHES ATTENUATORS AND LIMITERS

5082-3040/41
5082-3046
5082-3071
5082-3140/41
5082-3170
5082-3340





Features

HERMETIC
(5082-3140, 3141, 3170)

BROADBAND OPERATION
HF through X-band

LOW INSERTION LOSS
Less than 0.5 dB to 10 GHz (5082-3140, 3170)

HIGH ISOLATION
Greater than 20 dB to 10 GHz (5082-3140, 3170)

FAST SWITCHING/MODULATING
5 ns typical (5082-3141)

LESS DRIVE CURRENT REQUIRED
Less than 20 mA for 20 dB isolation (5082-3141)

Features

LOW COST TO USE
Designed for easy mounting

BROADBAND OPERATION
HF through Ku-band

LOW INSERTION LOSS
Less than 0.5 dB to 10 GHz (5082-3040, 3340)

LOW DRIVE CURRENT REQUIRED
Less than 20 mA for 20 dB isolation (5082-3041)

FAST SWITCHING MODULATION
5 ns typical (5082-3041)

HIGH POWER LIMITING
50 W peak pulse power (5082-3071)

Description

When forward biased these PIN diodes will appear as current variable resistors in shunt with a 50 ohm transmission line. The resistance varies between less than 1 ohm at high forward bias to greater than 10,000 ohms at zero or reverse bias.

The HP 5082-3040, -3046, -3340, -3140 and -3170 are passivated planar devices. The HP 5082-3041, -3071 and -3141 are passivated mesa devices. All of the devices are in a shunt configuration in stripline packages. These diodes are optimized for good continuity of characteristic impedance which allows a continuous transition when used in 50 ohm microstrip or stripline circuits.

Of these devices, the HP 5082-3040, -3041, -3046, -3071 and -3340 are in HP Package Outline 61.

The HP 5082-3140, -3141 and -3170 are in HP Package Outline 60. This package is hermetic and can be used for Hi-Rel applications. The HP 5082-3140, -3141 and -3170 are direct mechanical replacements for Outline 61 (with top cap in place) diodes HP 5082-3040, -3041, and -3340 respectively. The only electrical difference is the location of the chip in each package. Except in those few applications where the difference in phase relationship is important, the Outline 60 devices can be used as replacements.

The HP 5082-3071 passive limiter chip is functionally integrated into a 50 ohm transmission line to provide a broadband, linear, low insertion loss transfer characteristic for small signal levels. At higher signal levels self-rectification reduces the diode resistance to provide limiting as shown in Figure 6. Limiter performance is practically independent of temperature over the rated temperature range.

Applications

SWITCHES/ATTENUATORS

These diodes are designed for applications in microwave and HF-UHF systems using stripline or microstrip transmission line techniques.

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band.

These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3340 and 5082-3170 are reverse polarity devices with characteristics similar to the 5082-3040 and 5082-3140 respectively.

The 5082-3041 and 5082-3141 are recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for maximum attenuation is required.

The 5082-3046 has been developed for high peak pulse power handling as required in TR switches for distance measurement and TACAN equipment. The long effective minority carrier lifetime provides for low intermodulation products down to 10 MHz.

More information is available in HP Application Note 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

LIMITER

The 5082-3071 limiter module is designed for applications in telecommunication equipment, ECM receivers, distance measuring equipment, radar receivers, telemetry equipment, and transponders operating anywhere in the frequency range from 500 MHz through 10 GHz. An external dc return is required for self bias operation. This dc return is often present in the existing circuit, i.e. inductively coupled antennas, or it can be provided by a $\lambda/4$ resonant shunt transmission line. Selection of a high characteristic impedance for the shunt transmission line affords broadband operation. Another easy to realize dc return consists of a small diameter wire connected at a right angle to the electric field in a microstrip or stripline circuit. A 10 mA forward current will actuate the PIN diode as a shunt switch providing approximately 20 dB of isolation.

HP Package Outline 61 Cover Channel

The cover channel supplied with each diode should be used in balanced stripline circuits in order to provide good electrical continuity from the upper to the lower ground plane through the package base metal. Higher order modes will be excited if this cover is left off or if poor electrical contact is made to the ground plane.

The package transmission channel is filled with epoxy resin which combines a low expansion coefficient with high chemical stability.

Maximum Ratings at T_{CASE}=25°C

Part No. 5082-	-3140 -3170	-3141	-3040 -3340	-3041	-3046	-3071
Junction Operating and Storage Temperature Range	-65°C to 150°C	-65°C to 150°C	-65°C to 125°C	-65°C to 125°C		
Power Dissipation[1]	1.75 W	.75 W	2.5 W	1.0 W	4.0 W	1.0 W
Peak Incident Pulse Power[2]	225 W	50 W	225 W	50 W	2000 W	50 W
Peak Inverse Voltage	150 V	70 V	150 V	70 V	400 V	50 V
Soldering Temperature	230°C for 5 sec.					

Notes:
1. Device properly mounted in sufficient heat sink, derate linearly to zero at maximum operating temperature.
2. t_p = 1 μs, f = 10 GHz, Du = .001, Z_o = 50Ω. (Exception: -3071 is tested at 9.4 GHz.)

Electrical Specifications at T_A=25°C - Attenuator Diodes

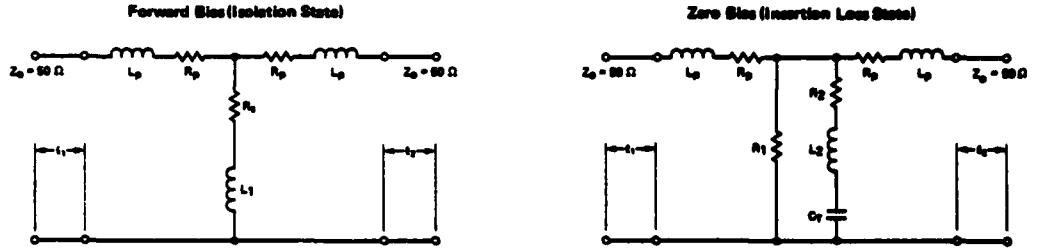
Part Number 5082-	Package Outline	Heat Sink	Minimum Isolation (dB)	Maximum Insertion Loss (dB)	Maximum SWR	Maximum Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
3140	61	Anode	20	0.5	1.5	–	400	30
3141	61	Cathode	20	1.0	1.5	10	15	13
3170	61	Cathode	20	0.5	1.5	–	400	30
3340	61	Anode	20	0.5	1.5	–	400	30
3041	61	Cathode	20	1.0	1.5	10	15	13
3046	61	Anode	20	1.0	1.5	–	1000	50
3340	61	Cathode	20	0.5	1.5	–	400	30
Test Conditions Note 3:	–	–	I_F=100mA (Except 3041,3141; I_F=20mA)	I_F = 0 P_{in} = 1mW	I_F = 0 P_{in} = 1mW	I_F = 20mA V_R = 10V Recovery to 90%	I_F = 50mA I_R = 250mA	–

Note 3: Test Frequencies: 8 GHz 5082-3041, -3046 and -3141. 10 GHz 5082-3040, -3140, 3170 and -3340.

Electrical Specifications at T_A=25°C - Limiter Diode

Part Number 5082-	Package Outline	Heat Sink	Maximum Insertion Loss (dB)	Maximum SWR	Maximum RF Leakage Power (W)	Typical Recovery Time (ns)
3027	61	Cathode	1.2	2.0	1.0	100
Test Conditions	–	–	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 50 W	P_{in} = 50 W

Equivalent Circuits



Typical Equivalent Circuit Parameters - Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L_1 (pH)	ℓ_1 (mm)	ℓ_2 (mm)
3040, 3340	200	0.25	1.0	20	2.4	5.0
3041	220	0.25	1.0	20	2.4	5.0
3046	220	0.25	0.6	17	2.4	5.0
3140, 3170	150	0.0	0.95	30	3.8	3.8
3141	150	0.0	0.8	20	3.8	3.8

Typical Equivalent Circuit Parameters - Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R_1 (KΩ)	L_2 (pH)	R_2 (KΩ)	C_T (pF)	ℓ_1 (mm)	ℓ_2 (mm)
3040, 3340	200	0.25	∞	0	5.0	0.10	2.4	5.0
3041	220	0.25	∞	0	1.5	0.15	2.4	5.0
3046	220	0.25	∞	0	1.5	0.15	2.4	5.0
3140, 3170	30	0.0	1.2	16	0.0	0.20	5.3	5.3
3141	200	0.0	∞	0	0.4	0.14	4.4	4.4

Typical Parameters

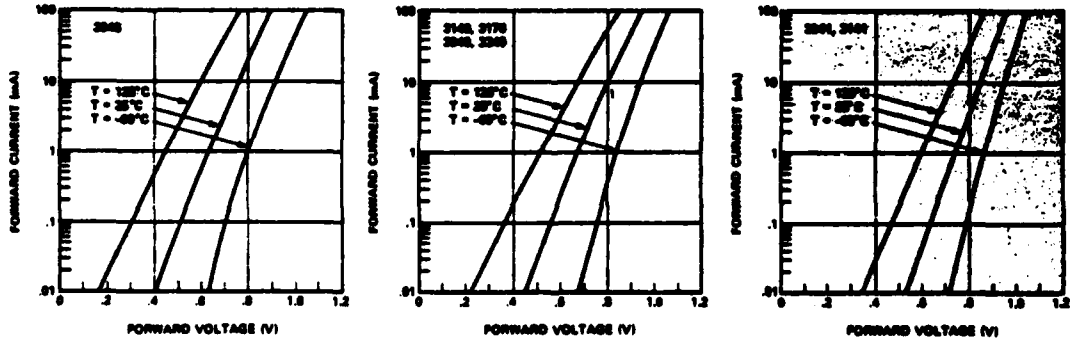


Figure 1. Typical Forward Characteristics

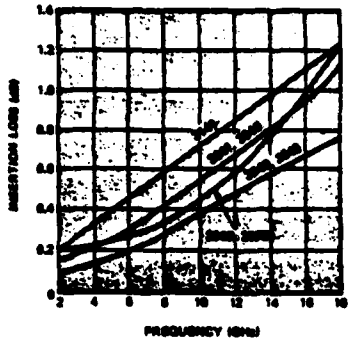


Figure 2. Typical Insertion Loss vs. Frequency.

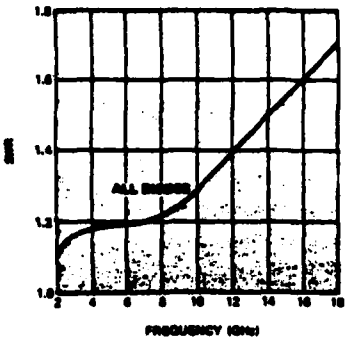


Figure 3. Typical SWR vs. Frequency.

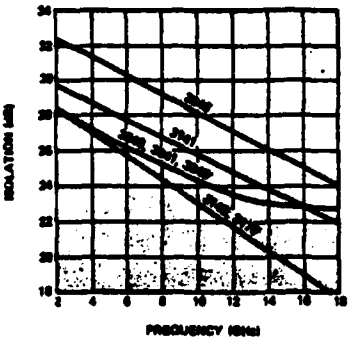


Figure 4. Typical Isolation vs. Frequency.

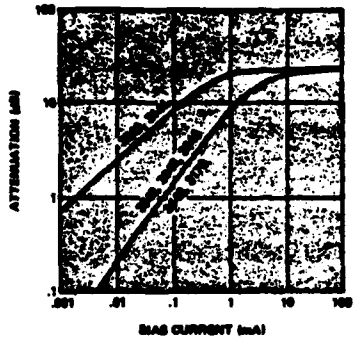


Figure 5. Typical Attenuation Above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.

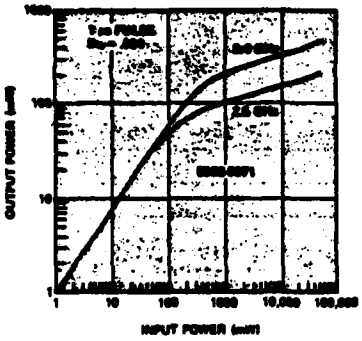
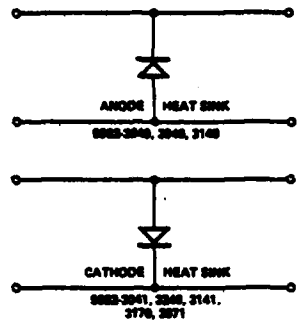


Figure 6. Typical Pulse Limiting Characteristics.



HEAT SINK POLARITY

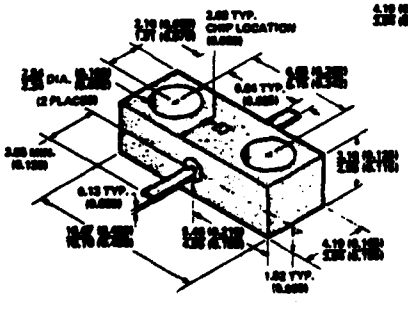


Figure 7. HP Package 60 Outline.

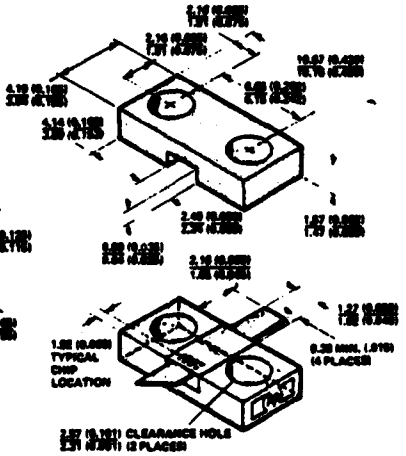


Figure 8. HP Package 61 Outline.

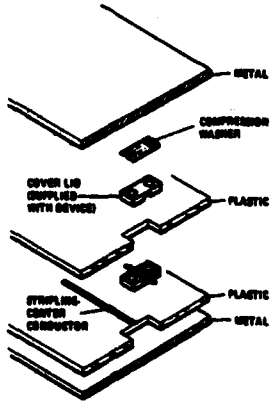


Figure 9. Suggested Stripline Assembly.

Typical Switching Parameters

RF SWITCHING SPEED

HP 5082-3141 and HP 5082-3041

The RF switching speed of the HP 5082-3141 and HP 5082-3041 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50Ω system is considered for two cases: one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second, driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 10. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

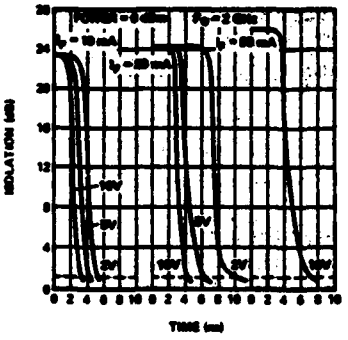


Figure 10. Isolation vs. Time (Turn-on) for HP 5082-3141 and HP 5082-3041. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929; Fast Switching PIN Diodes.

REVERSE RECOVERY TIME

Shown below is reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_R. The circuit used to measure t_{rr} is shown in Figure 11.

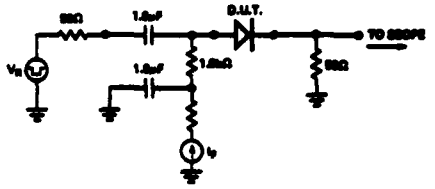


Figure 11. Basic t_{rr} Test Setup.

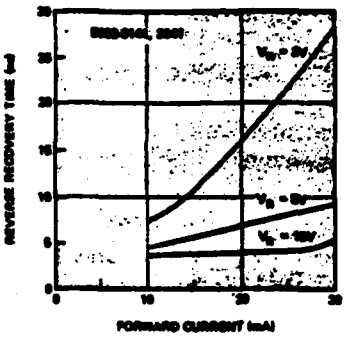


Figure 12. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3141, -3041.

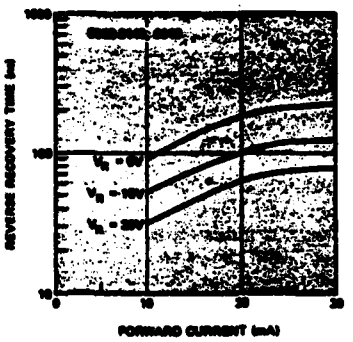


Figure 13. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3140, -3040.

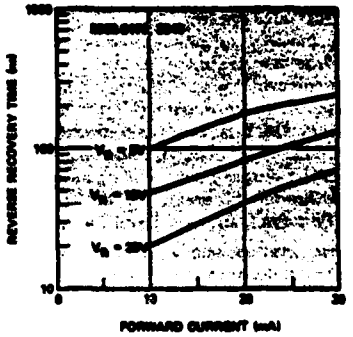
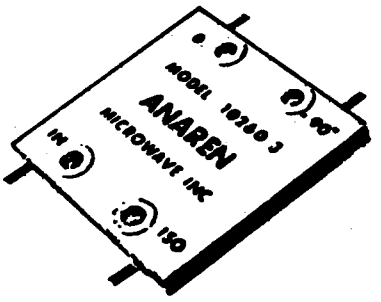


Figure 14. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3178, -3348.

Anaren

Hybrid Couplers 3 dB, 90° Ultra-Miniature



Features

For installation directly in microstrip circuits
Largest selection of frequency ranges and case styles
Lowest cost
Smallest size, lightest weight
Laminated stripline construction
High isolation with low VSWR
Rugged aluminum cases
Meets MIL-E-5400 Class 3 requirements

Description

This ultra-miniature series of 3 dB, 90° hybrid couplers is available in 34 standard models and 15 case styles to cover the frequency range 30 MHz to 4.0 GHz. The popular 225-400 MHz band is covered by 4 standard case styles.

Anaren ultra-miniature, 3 dB, 90° hybrid couplers are well suited for a variety of applications: power dividers and combiners, balanced amplifier circuits with low input and output VSWR, matrix amplifiers, voltage variable PIN diode attenuators, balanced mixers and modulators, switching networks, balanced detectors, antenna feed networks and phase shifters and comparators.

There are a number of techniques available for constructing microwave quadrature hybrids, but Anaren uses the backward wave 3 dB, 90° hybrid coupler in stripline form. This stripline version is smaller, provides better performance and can cover wider bandwidths than other types. The single-section, backward wave, 3 dB hybrid allows octave bandwidth coverage and multi-section versions can easily be designed to cover multi-octave and decade bandwidths.

Applications

Inexpensive power dividers and combiners
Low cost balanced amplifier designs
Matrix amplifiers
Voltage variable PIN diode attenuators
Balanced mixers and modulators
Switching networks
Balanced detectors
Antenna feed networks
Phase shifters and comparators

All Anaren ultra-miniature couplers are printed on stable teflon-glass substrates using shielded stripline techniques. They are laminated under heat and pressure using a low loss dielectric bonding compound. The package assures high reliability and is capable of withstanding extreme environmental stress.

The couplers are designed to mate with 30 mil microstrip and mounting holes are provided for attaching the coupler ground plane. A reliable electrical ground contact is necessary for optimum performance.

The Anaren ultra-miniature coupler is a reciprocal four-port network.

An input signal applied to any port (port 1, for example) will divide equally to the two opposite ports (3 and 4) with port 2 remaining isolated. The voltage at port 4 lags the voltage at port 3 by 90°. This phase quadrature relationship is independent of frequency and is the unique property which makes the 90° coupler so versatile.

See pages 45 and 71 for additional information.

Electrical Specifications

Model No.	Frequency (GHz)	Isolation Min/Typ (dB)	VSWR Max/Typ	Insertion Loss Max (dB)	Amplitude Balance Max (dB)	Phase Balance (deg)	Case Style
10230-3	.030-.076	15/20	1.40/1.20	0.35	±0.75	±1.5	102
10270-3	.030-.076	20/25	1.20/1.10	0.35	±0.75	±1.5	103
1A0270-3	.040-.080	20/25	1.20/1.10	0.30	±0.50	±1.5	103
1A0230-3	.054-.088	20/22	1.20/1.10	0.35	±0.50	±1.5	102
10261-3	.0625-.125	20/27	1.20/1.10	0.35	±0.50	±1.5	104
1A0280-3	.090-.180	20/27	1.20/1.10	0.30	±0.50	±1.5	104
1H0280-3	.090-.180	18/25	1.20/1.10	0.30	±0.50	±1.5	116
1B0261-3	.100-.200	20/25	1.20/1.10	0.30	±0.50	±1.5	104
1J0280-3	.100-.160	20/27	1.20/1.10	0.30	±0.30	±1.5	116
1A0920-3	.100-.500	16/20	1.35/1.15	0.50	±0.60	±2.0	117A
10280-3	.116-.150	20/27	1.20/1.10	0.30	±0.30	±1.5	104
10262-3	.125-.250	20/27	1.20/1.10	0.30	±0.50	±1.5	105
10260-3	.225-.400	20/25	1.20/1.10	0.30	±0.50	±1.5	106
1A0260-3	.225-.400	20/25	1.20/1.10	0.30	±0.50	±1.5	107
1B0260-3	.225-.400	20/25	1.20/1.10	0.30	±0.50	±1.5	108
1R0260-3	.225-.400	20/25	1.20/1.10	0.30	±0.50	±1.5	110
1S0260-3	.225-.400	20/25	1.20/1.10	0.30	±0.50	±1.5	106
1H0263-3	.250-.500	20/22	1.20/1.10	0.30	±0.50	±1.5	110
10263-3	.250-.500	20/25	1.20/1.10	0.30	±0.50	±1.5	106
1D0263-3	.300-.550	20/25	1.20/1.10	0.30	±0.50	±1.5	106
1A0263-3	.400-.600	20/25	1.20/1.10	0.30	±0.50	±1.5	106
1B0263-3	.400-.700	20/25	1.20/1.10	0.30	±0.50	±1.5	108
1H0264-3	.440-.880	20/25	1.20/1.10	0.30	±0.50	±1.5	111A
10264-3	.500-1.0	20/25	1.20/1.10	0.30	±0.50	±1.5	111
1B0264-3	.500-1.0	20/25	1.20/1.10	0.30	±0.50	±1.5	112
1A0264-3	.600-1.2	20/25	1.20/1.10	0.30	±0.50	±1.5	111
10330-3	.700-1.4	20/25	1.25/1.10	0.30	±0.50	±1.5	113
10890-3	.950-1.225	20/25	1.25/1.15	0.30	±0.30	±1.5	112
10265-3	1.0-2.0	20/24	1.25/1.10	0.30	±0.50	±1.5	113
1B0265-3	1.0-2.0	20/24	1.25/1.15	0.30	±0.50	±1.5	112
1E0320-3	1.3-2.6	20/25	1.30/1.15	0.30	±0.50	±2.0	113
10320-3	1.7-2.5	20/23	1.30/1.20	0.30	±0.50	±1.5	113
1B0320-3	1.7-2.5	20/25	1.30/1.15	0.30	±0.50	±1.5	112
10266-3	2.0-4.0	18/21	1.30/1.20	0.30	±0.50	±2.0	114

Power: 200 W @ 85°C. Derate to 100 W @ 100°C.
Derate to Zero Watts @ 150°C.

Power rating applies when solder tab/coupler interface has been conformally coated to eliminate voltage breakdown.

Nominal Impedance: 50 ohms, non-reactive.

These specifications apply for tests performed with properly designed microstrip test fixtures.

Couplers meet environmental requirements of MIL-E-5400, Class 3; as applicable.

Specifications subject to change without notice

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